Design a circuit that has two inputs, clk and X, and produces one output O. X may change every clock cycle, and the change happens at the falling edge. The circuit samples the input at every rising edge of the clock. If the input is 1, consider as read a 1, else read a 0. O is 1 (for one clock cycle, from positive edge to positive edge) if the last three bits read are 011 (0 is the least recent bit).

1. Draw the state diagram. Close to an arc, show X=1 or X=0 to indicate whether the change of state happens when X=1 or when X=0.

S0: got nothing

S1: got 0

S2: got 01

S3: got 011

X=0

X=0

X=1

X=0

X=0

X=1

X=1

X=1

1. Assign S0 to 00, S1 to 01, S2 to 10, and S3 to 11.Draw the next-state table, and derive the functions for D1 and D0. Derive the output function. Finish the Verilog module for this circuit.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q1** | **Q0** | **X** | **D1** | **D0** |
| 0 | 0 | 0 |  0 | 1  |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 |

D1

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  Q1Q0 X  | 00 | 01 | 11 | 10 |
| 0 |  |  |  |  |
| 1 |  | 1 |  | 1 |

D0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  Q1Q0 X  | 00 | 01 | 11 | 10 |
| 0 | 1 | 1 | 1 | 1 |
| 1 |  |  |  | 1 |

module seqdector (clk, X, O);

 input clk, X;

 output O;

 wire D1, D0, Q1, Q0, Q1bar, Q0bar;

 assign D0 = ~X | (Q1&~Q0);

 Dff1 C0 (D0, clk, Q0, Q0bar);

 assign D1 = (~Q1&Q0&X) | (Q1&~Q0&X);

 Dff1 C1 (D1, clk, Q1, Q1bar);

 assign O = Q1 & Q0;

endmodule