**Assignment #5 – Digital Logic Design I – Combinational Logic**

CDA 3100, Computer Organization I

Note: The instructions of how to download the ModelSim software are in the slides.

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**Problem 1 (50 points)** Design a circuit that takes three bits X2, X1, X0, as input, and output one bit O as output. O is 1 if and only if 5<=X<=7 when X=(X2, X1, X0) is read as an unsigned integer.

1. Construct the truth table.

|  |  |  |  |
| --- | --- | --- | --- |
| X2 | X1 | X0 | O |
| 0 | 0 | 0 |  |
| 0 | 0 | 1 |  |
| 0 | 1 | 0 |  |
| 0 | 1 | 1 |  |
| 1 | 0 | 0 |  |
| 1 | 0 | 1 |  |
| 1 | 1 | 0 |  |
| 1 | 1 | 1 |  |

1. Write down the sum-of-product form of the function without any simplification in the form as: O = (X2 & X1 & X0) | (~X2 & X1 & X0) | … (this is NOT the answer).
2. Simplify the circuit using Karnaugh-map.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  X2X1 X0  | 00 | 01 | 11 | 10 |
| 0 |  |  |  |  |
| 1 |  |  |  |  |

1. Write down the Verilog module for this circuit called module HW5P1 (X2, X1, X0, O).

module HW5P1 (X2, X1, X0, O);

endmodule

1. A Verilog code has been provided for this homework with an empty HW5P1 module. Please replace this module with your module and run simulation. Copy and paste the waveform **only related to this problem** here. (One way to copy and paste is (1) print screen (2) paste the screen to the windows paint program (3) crop the waveform (4) paste it here.).

**Problem 2 (50 points)** Design a circuit that takes three bits A, B, S as input, and output one bit O as output. If S=0, O=A|B. If S=1, O=A&B.

1. Construct the truth table.

|  |  |  |  |
| --- | --- | --- | --- |
| S | A | B | O |
| 0 | 0 | 0 |  |
| 0 | 0 | 1 |  |
| 0 | 1 | 0 |  |
| 0 | 1 | 1 |  |
| 1 | 0 | 0 |  |
| 1 | 0 | 1 |  |
| 1 | 1 | 0 |  |
| 1 | 1 | 1 |  |

1. Write down the sum-of-product form of the function without any simplification in the form as: O = (A &B&S) |(A &B&~S) | … (this is NOT the answer)
2. Simplify the circuit using Karnaugh-map.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  SA B  | 00 | 01 | 11 | 10 |
| 0 |  |  |  |  |
| 1 |  |  |  |  |

1. Write down the Verilog module for this circuit called module HW5P2 (S,A,B,O).

module HW5P2 (S,A,B,O);

endmodule

1. A Verilog code has been provided for this homework with an empty HW5P2 module. Please replace this module with your module and run simulation. Copy and paste the waveform **only related to this problem** here. (One way to copy and paste is (1) print screen (2) paste the screen to the windows paint program (3) crop the waveform (4) paste it here.).

**Extra Point Problem 1 (10 points)** The following is the 1-bit ALU we discussed in the class that can support and, or, add, and sub. Please simplify the design by replacing the circuit in the red box with exactly one gate with 2 inputs and 1 output.



**Extra Point Problem 2 (10 points)** We talked about multiplexors (selector) in the class. A 4-1 multiplexor has 6 inputs: S1, S0, d3, d2, d1, and d0, as well as one output, O. It works as follows

* If S1S0=00, O=d0.
* If S1S0=01, O=d1.
* If S1S0=10, O=d2.
* If S1S0=11, O=d3.

Show how to use only one 4-1 multiplexor (no any other gates should be used, including the inverter, meaning that the inputs to the 4-1 multiplexor can only come from A, B, C, 0, and 1) to implement function F(A,B,C) with truth table as follows. **Please finish the following figure, showing each input of the 4-1 multiplexor is connected to what input value, as your answer. No Verilog code or simulation is needed.**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **C** | **Output** |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

