Study Guide for Final Exam – CDA 3100 Computer Organization

1, Single cycle datapath and control

(1) Know datapath for R-format instructions: participated elements and data flow
(2) Know control signal setting for R-format instructions
(3) Know datapath for I-format instructions (lw and sw): participated elements and data flow
(4) Know control signal setting for I-format instructions
(5) Know datapath for branch instruction: participated elements and data flow
(6) Know control signal setting for the branch instruction
(7) Know datapath for J-format instruction: participated elements and data flow
(8) Know control signal setting for J-format
(9) Know how the control signals control the datapath: RegDst, ALUSrc, ALUop, RegWrite, MemRead, MemWrite, MemtoReg, Branch, and jump
(10) Given descriptions of the new instructions, know the datapath and control signal settings.

2, Pipeline

(1) Know the five stages in the pipeline datapath
(2) For R-format, lw, and branch instructions, know the datapath and controls in each stage.
(3) Know the functions of pipeline registers and how pipeline registers help forward data
(4) Know how to find dependencies between instructions on a specific register
(5) For each pair of dependency, know whether there is a data hazard
(6) For the potential data hazard, know how to forward data and whether stall is needed.
(7) Know how to detect and handle data hazard: hazard detection unit, forwarding unit.
(8) Know how to detect control hazard. (ID stages)
(9) Know what happens to the instructions and pipelines when a control hazard is detected.
(10) Know three solutions to control hazard: assuming branch not taken, performing branching in the ID stage, and dynamic branch prediction (1-bit branch prediction buffer, 2-bit branch prediction buffer, and branch target buffer).
(11) Know what happens to the instructions and pipelines when an exception is detected.

3, Memory hierarchy

(1) Know the memory hierarchy structure
(2) Know three types of caches, direct-mapped cache, set-associative caches, and full-associative caches, as well as their differences.
(3) Know the partition of a physical address. (Tag, index, and byte offset)
(4) For each type of cache, know how to index into cache block given a physical address.
(5) Know the fields of each cache block: valid bit, tag, data. If the cache is TLB, data is the physical page number
(6) Know how to read data from cache: whether we need to visit main memory or not, whether we need to update cache or not.
(7) Know how to write data to cache given an address: write-through, write-back
(8) Know how to write data if the block to be written is not in the cache: write-allocate, no-write allocate.

(9) Know how to divide up a virtual address so that it can index into the TLB cache. (TLB tag, TLB index, page offset)
(10) Know how to divide up a virtual address so that it can index into the page table. (virtual page number, page offset)
(11) Know how to divide up a physical address in virtual system. (physical page number, page offset)
(12) Know how to translate virtual address to physical address.
(13) Know what TLB and page table are, as well as how they help translate virtual address to physical address.
(14) Given a virtual address, how to find the physical address

4, Parallel

(1) Know what the multicore processor is.
(2) Know three levels of parallelism
(3) Know the vector architecture for SIMD and vector processing
(4) Know what the multithreading is and three types of multithreading
(5) Know what the GPU is.
(6) Know what the WSC is.

5, Security

(1) Know the goals of computer security
(2) Know the stack smashing
(3) Know the defensive approaches to the attack due to stack smashing