Concepts Introduced

- Introduction
- Number Representation
- Assembly 1
- Assembly 2

Computer Measurement

- Execution time
- Performance
- Clock period and clock rate
- CPU time, CPI (cycles per instruction)
- Amdahl's Law

Performance Equations

• Performance has an inverse relationship to execution time.

$$Performance = \frac{1}{Execution_Time}$$

• Comparing the performance of two machines can be accomplished by comparing execution times.

 $Performance_X > Performance_Y$

$$\frac{1}{Execution_Time_X} > \frac{1}{Execution_Time_Y}$$

$$Execution_Time_Y > Execution_Time_X$$

N Times Faster

• Often people state that a machine X is *n* times faster than a machine Y. What does this mean?

$$\frac{Performance_X}{Performance_Y} = n = \frac{Execution_Time_Y}{Execution_Time_X}$$

• If machine X takes 20 seconds to perform a task and machine Y takes 2 minutes to perform the same task, then machine X is how many times faster than machine Y?

Measures of Clock Speed

- clock periods
 - millisecond (ms) 10^{-3} of a second
 - microsecond (μ s) 10⁻⁶ of a second
 - nanosecond (ns) 10^{-9} of a second
 - picosecond (ps) 10^{-12} of a second
 - femtosecond (fs) 10^{-15} of a second
- clock rates
 - kilohertz (KHz) 10^3 cycles per second
 - megahertz (MHz) 10^6 cycles per second
 - gigahertz (GHz) 10^9 cycles per second
 - terahertz (THz) 10^{12} cycles per second
 - petahertz (PHz) 10^{15} cycles per second
- If the clock period for a computer is 2ns, then what is its clock rate?
- Why do computer manufacturers quote clock rates instead of clock periods?

Measures of Data Size

- bit Binary digIT
- nibble four bits
- byte eight bits
- word often four bytes (32 bits) on many embedded/mobile processors and eight bytes (64 bits) on many desktops and servers
- kibibyte (Kib) [kilobyte (Kb)] 2¹⁰ (1,024) bytes
- mebibyte (Mib) [megabyte (Mb)] 2²⁰ (1,048,576) bytes
- gibibyte (Gib) [gigabyte (Gb)] 2³⁰ (1,073,741,824) bytes
- tebibyte (Tib) [terabyte (Tb)] 2⁴⁰ (1,099,511,627,776) bytes
- pebibyte (Pib) [petabyte (Pb)] 2⁵⁰ (1,125,899,906,842,624) bytes

CPU Time

- CPU time ignores I/O and the time for executing other processes.
- CPI stands for cycles per instruction.

 $CPU_time = CPU_clock_cycles * clock_cycle_time = \frac{CPU_clock_cycles}{clock_rate}$ $CPI = \frac{CPU_clock_cycles}{instruction_count}$

CPU_time = Instruction_count * CPI * clock_cycle_time

• Suppose two implementations of the same ISA are executing the same program. Computer A has a clock cycle time of 250ps and a CPI of 2.0. Computer B has a clock cycle time of 500ps and a CPI of 1.2. Which computer is faster and by how much?

CPU Time (cont.)

- CPI cannot be looked up in a manual as it can be affected by many external events.
 - Pipelines can be flushed.
 - Branch information can be replaced in various buffers (BPB, BTB).
 - Page translation information can be evicted (ITLB, DTLB).
 - Blocks of data or instructions can be evicted from cache or memory.
- CPU time really needs to be measured and it can vary somewhat on each execution.

Amdahl's Law

• Amdahl's Law states that the performance improvement to be gained from using some faster mode of execution is limited by the fraction of the time the faster mode can be used.



Amdahl's Law

- Amdahl's Law depends on two factors:
 - The fraction of the time the enhancement can be exploited.
 - The improvement gained by the enhancement while it is exploited.

 $speedup_{overall} = rac{execution_time_{old}}{execution_time_{new}} = rac{1}{(1 - fraction_{enhanced}) + rac{fraction_{enhanced}}{speedup_{enhanced}}}$ $execution_time_{new} = execution_time_{old} * (1 - fraction_{enhanced} + rac{fraction_{enhanced}}{speedup_{enhanced}})$

• If the speed of a CPU is improved by a factor of 5 and the CPU requires 40% of the machines execution time, then what is the overall speedup?

$$\frac{1}{1 - 0.4 + \frac{0.4}{5}}$$

Commonly Used Bases

• Which base is commonly used for computers and why?

Base	Name	Digits	Example
10	Decimal	0-9	5023 ₁₀
2	Binary	0-1	10011100111112
8	Octal	0-7	11637 ₈
16	Hexadecimal	0-9,a-f	$139f_{16}$

Number Representation

Assembly 2 00000000000

Binary Number Representation

- The binary representation contains two symbols: { 0, 1 }
- Position of each symbol represents a power of two $d_nd_{n-1}...d_1d_0.d_1...d_m = d_n \times 2^n + d_{n-1} \times 2^{n-1} + ... + d_1 \times 2^1 + d_0 \times 2^0$ $+ d_{-1} \times 2^{-1} + d_{-2} \times 2^{-2} + ... + d_m \times 2^{-m}$ $= \sum_{i=-m}^n d_i \times 2^i$
- What is the value of the binary representation 111?

	1	1	1	
	↑	↑	↑	
position:	2	1	0	
111 = 1×2 = 1×4 = 4 +	2 + 1> + 1× 2 + 1	<2 ¹ + 1 2 + 1ב = 7	×2º 1	

• It is also the way to convert binary number to decimal number.

Conversion from Decimal to Binary Number

- Converting from decimal to binary (before the decimal point):
 - Repeatedly divide it by 2, until the quotient is 0.
 - Write down the remainder, the last remainder first.
- Example:

```
(458)_{10} = (?)_2
              remainder 0
                               MSB
458 / 2 = 229
229 / 2 = 114
              remainder 1
114/2 = 57
              remainder 0
 57 / 2 = 28 remainder <sup>Zoom</sup>
 28/2 = 14
             remainder 0
 14/2 =
              remainder 0
          7
  7/2=
          3
              remainder 1
  3 / 2 = 1 remainder 1
     LSB
```

Conversion from Decimal to Binary Number (cont.)

- Converting from decimal to binary (After the decimal point):
 - Multiply the fractional part including decimal point by 2 until the first digit after decimal point becomes 0.
 - Write down the integral part, the first remainder first.
- Example

 $(458.692)_{10} = (?)_2$ $.692 \times 2 = 1.384 | 1 \text{ MSB} \\ .384 \times 2 = 0.768 \\ .768 \times 2 = 1.536 \\ .536 \times 2 = 1.072 | 1 \text{ LSB}$ So: $(458.692)_{10} = (111001010.1011)_2$

Conversion between Binary and Hexadecimal Number

- Extremely easy.
 - From base 2 to base 16: divide the digits into groups of 4, then apply the table.
 - From base 16 to base 2: replace every digit by a 4-bit string according to the table.
- Because 16 is 2 to the power of 4.
- Examples:

base 2 to base 16

base 16 to base 2

0001010111011001 → 0001₂0101₂1101₂1001₂ →1₁₆5₁₆D₁₆9₁₆ →15D9₁₆ A2D4₁₆

 $\rightarrow A_{16} 2_{16} D_{16} 4_{16}$

- → $1010_20010_21101_20100_2$
- →1010001011010100

Unsigned and Signed Integers

- Unsigned integers: non-negative numbers Binary representation: $d_{n-1}d_{n-2}\cdots d_1d_0 = d_{n-1} * 2^{n-1} + d_{n-2} * 2^{n-2} + \cdots + d_1 * 2^1 + d_0 * 2^0$
- Signed integers:
 - Non-negative integers: MSB is 0
 - Negative integers: MSB is 1

Two's complement representation: $d_{n-1}d_{n-2}\cdots d_1d_0 = -d_{n-1} * 2^{n-1} + d_{n-2} * 2^{n-2} + \cdots + d_1 * 2^1 + d_0 * 2^0$

Introduction

Two's Complement Negation

• Negation of a two's compliment number is accomplished by inverting the bits and adding 1.

$$x + \overline{x} = 111...111 = -1$$
$$x + \overline{x} + 1 = 0$$
$$\overline{x} + 1 = -x$$

• Example 1:

$$= -3_{10}$$

• Example 2:

- - $= 00000000000000000000000000011_2$

 $= 3_{10}$

Binary Addition

• Rules: add the values and discard any carry-out bit

Examples: using 8-bit two's complement numbers.

1. Add -8 to +3

(+3)	0000	0011
+(-8)	1111	1000
(-5)	1111	1011

2. Add -5 to -2

Binary Subtraction

• Rules: if we consider A – B, we first negate B and add it to A and discard any carry-out bit

Example: Using 8-bit Two's Complement Numbers ($-128 \le x \le +127$)

(+8) 0000 1000 0000 1000 -(+5) 0000 0101 -> Negate -> +1111 1011 ----- (+3) 1 0000 0011 : discard carry-out

Detecting Overflow

- Overflow occurs when the result of performing an arithmetic operation is not within the range of representable values.
- Overflow on addition only occurs when the MSBs of the operands are the same and the MSB of the result differs.

A + B			
Operand A	Operand B	Result	Overflow?
≥ 0 < 0	≥ 0 < 0	< 0 ≥ 0	Yes
≥ 0 < 0	≥ 0 < 0	≥ 0 < 0	No
$ \begin{array}{c} \geq 0 \\ \geq 0 \\ < 0 \\ < 0 \end{array} $		$ \begin{array}{c} < 0 \\ \ge 0 \\ < 0 \\ \ge 0 \end{array} $	No No No No

Introduction

Number Representation

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Overflow for Addition

Example: Using 4-bit Two's Complement numbers ($-8 \le x \le +7$)

(-7) 1001
+(-6) 1010
-----(-13) 1 0011 = 3 : Overflow (largest -ve number is -8)

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Number Representation

Assembly 2 00000000000

Overflow for Subtraction

Example: Using 4-bit Two's Complement numbers ($-8 \le x \le +7$)

```
Subtract -6 from +7
```

(+7) 0111 0111 -(-6) 1010 -> Negate -> +0110 -----13 1101 = -8 + 5 = -3 : Overflow

Assembly 2 0000000000

Zero Extension – Extending to a Larger Unsigned Representation

- Converting an unsigned value to a larger representation is called zero extension.
- Zero extension is accomplished by filling in the new bits of the larger representation with zero.

C Type Number		Decimal
unsigned char	10010110	150
unsigned short	000000010010110	150
unsigned int	0000000000000000000000000000010010110	150

Sign Extension – Extending to a Larger Two's Complement Representation

- Converting a two's complement value to a larger representation is called sign extension.
- Sign extension is accomplished by taking the most significant bit from the value in the smaller representation and replicating it to fill in the new bits of the larger representation.

C Type	Number	Decimal
char	00000011	3
short	00000000000011	3
int	000000000000000000000000000000000000000	3
char	11111101	-3
short	1111111111111111	-3
int	111111111111111111111111111111111111111	-3

Scientific Notation

- Scientific notation uses 3 integers to represent values. representation.
 - radix (or base) r
 - significand (or mantissa) s
 - exponent x
- The standard form is:
 - *s* * *r*[×]
- 15.625 can be represented as:
 - 15.625 * 10⁰
 - 1.5625 * 10¹
 - 15625 * 10⁻³

IEEE 754 Floating-Point Standard

- A standard for floating-point representation called the IEEE 754 Floating-Point Standard (FPS) is now widely used.
 - Programs become more portable since the results of floating-point operations are similar across different machines.
 - Floating-point data can be transferred from one machine to another without performing conversions.
- Below is the format used for representation of single precision floating-point values in the IEEE FPS, where S is the sign bit, E is a biased exponent, and F represents the bits of the significand with the leading bit hidden.



IEEE 754 Floating-Point Standard (cont.)



• Below is how the IEEE FPS format is interpreted.

$$(-1)^{S} * (1 + 0.F) * 2^{(E-127)}$$

- The 1 is added to 0.F to make the leading bit of normalized binary numbers implicit and save a bit of space. This is referred to as the hidden bit.
- The E is adjusted by a bias of 127. Positive exponents will have larger unsigned biased value than negative exponents. This makes it easier to determine the larger magnitude of two IEEE FPS values (The larger the E, the larger the magnitude).

Example of Representing a Value in IEEE FPS

- Determine the hexadecimal IEEE FPS pattern that represents the decimal value 9.5.
- IEEE FPS pattern: $(-1)^{S} * (1 + 0.F) * 2^{(E-127)}$

```
9.5_{10} = 1001.1_2
= 1.0011<sub>2</sub> * 2<sup>3</sup>
= (-1)<sup>0</sup> * (1 + 0.0011<sub>2</sub>) * 2<sup>(130-127)</sup>
= (-1)<sup>S</sup> * (1 + 0.F) * 2<sup>(E-127)</sup>
```

FPS = S E F

- $= 0 \ 10000010_2 \ 0011000000000000000000_2$
- $= 0100_2 \ 0001_2 \ 0001_2 \ 1000_2 \ 0000_2 \ 0000_2 \ 0000_2 \ 0000_2$
- $=41180000_{16}$

Example of Representing a Value in IEEE FPS (cont.)

- Determine the hexadecimal IEEE FPS pattern that represents the decimal value -6.25.
- IEEE FPS pattern: $(-1)^{S} * (1 + 0.F) * 2^{(E-127)}$

$$\begin{aligned} -6.25_{10} &= -110.01_2 \\ &= -1.1001_2 * 2^2 \\ &= (-1)^{-1} * (1 + 0.1001_2) * 2^{(129 - 127)} \\ &= (-1)^S * (1 + 0.F) * 2^{(E - 127)} \end{aligned}$$

FPS = S E F

- $= 1 \ 10000001_2 \ 10010000000000000000000_2$
- $= 1100_2 \ 0000_2 \ 1100_2 \ 1000_2 \ 0000_2 \ 0000_2 \ 0000_2 \ 0000_2$
- $= c0c80000_{16}$

Example of Determining an IEEE FPS Pattern Value

• Determine what decimal value that 0xc0900000₁₆ represents in the IEEE FPS.

 $FPS = c0900000_{16}$ = 1100_2 0000_2 1001_2 0000_2 0000_2 0000_2 0000_2 = 1 10000001_2 001000000000000000_2 = S E F

value =
$$(-1)^{S} * (1 + 0.F) * 2^{(E-127)}$$

= $(-1)^{1} * (1 + 0.001_{2}) * 2^{(129-127)}$
= $(-1) * (1.001_{2}) * 2^{2}$
= -100.1_{2}
= -4.5_{10}

Example of Determining an IEEE FPS Pattern Value (cont.)

• Determine what decimal value that $0 \times 40580000_{16}$ represents in the IEEE FPS.

 $FPS = 40580000_{16}$ = 0100₂ 0000₂ 0101₂ 1000₂ 0000₂ 0000₂ 0000₂ 0000₂ = 0 10000000₂ 1011000000000000000000 = S E F

value =
$$(-1)^{5} * (1 + 0.F) * 2^{(E-127)}$$

= $(-1)^{0} * (1 + 0.1011_{2}) * 2^{(128-127)}$
= $1 * (1.1011_{2}) * 2^{1}$
= 11.011_{2}
= 3.375_{10}

Instructions for a Machine

- A high-level language statement is typically represented by several assembly instructions.
- An assembly instruction is generally a symbolic representation of a machine instruction.
- A machine instruction is a set of bits representing a basic operation that a machine can perform.
- An instruction set is the set of possible machine instructions for a specific machine.

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 Assembly 2 00000000000

Example of Compilation Process



MIPS Assembly File

- A MIPS assembly file consists of a set of lines.
- Each line can be:
 - directive
 - instruction
- Each directive or instruction can start with a label, which provides a symbolic name for a data or instruction location.
- Each line can include a comment, which start with a # character and continues to the end of the line.

General Form of a MIPS Assembly Language Program

• All directives and instructions are placed on separate lines.

.data <declarations of variables> .text .globl main main: <instructions> jr \$ra # instruction indicating a return

MIPS Integer Registers

• There are only 32 MIPS integer (general-purpose) registers.

Name	Number	Usage	Callee Must Preserve?
\$zero	\$0	hardwired constant value zero	N/A
\$at	\$1	reserved for use by assembler	no
\$v0-\$v1	\$2-\$3	values for function results and expression evaluation	no
\$a0-\$a3	\$4-\$7	function arguments	no
\$t0-\$t7	\$8-\$15	temporaries	no
\$s0-\$s7	\$16-\$23	saved temporaries	yes
\$t8-\$t9	\$24-\$25	more temporaries	no
\$k0-\$k1	\$26-\$27	reserved for use by OS kernel	N/A
\$gp	\$28	global pointer	yes
\$sp	\$29	stack pointer	yes
\$fp	\$30	frame pointer	yes
\$ra	\$31	return address	yes

Introduction

lumber Representation

MIPS Directives

directive	meaning	
.align <i>n</i>	Align next datum on 2^n boundary.	
.asciiz <i>str</i>	Place the null-terminated string <i>str</i> in memory.	
.byte b1,,bn	Place the <i>n</i> byte values in memory.	
.data	Switch to the data segment.	
.double <i>d1,,dn</i>	Place the <i>n</i> double precision values in memory.	
.extern <i>sym size</i>	Declare that the datum stored at <i>sym</i> is <i>size</i> bytes and is a global label.	
.float f1,,fn	Place the <i>n</i> single precision values in memory.	
.globl sym	The label <i>sym</i> can be referenced in other files.	
.half <i>h1,,hn</i>	Place the <i>n</i> halfword values in memory.	
.space n	Allocates n bytes of space at the current location in the current segment.	
.text	Switch to the text segment.	
.word w1,,wn	Place the <i>n</i> word values in memory.	

QtSpim Syscalls

- Syscalls provide operating system services.
- $\bullet\,$ QtSpim input/output (I/O) and exit occurs through syscalls.

Service	Call Code Arg	Other Arguments	Result
print_int	v0 = 1	\$a0 = integer	
print_float	\$v0 = 2	\$f12 = float	
print_double	\$v0 = 3	\$f12 = double	
print_string	v0 = 4	\$a0 = string address	
read_int	\$v0 = 5		integer in \$v0
read_float	\$v0 = 6		float in \$f0
read_double	\$v0 = 7		double in \$f0
read_string	\$v0 = 8	\$a0 = string address \$a1 = max length	
exit	\$v0 = 10		
print_char	\$v0 = 11	\$a0 = char	
read_char	\$v0 = 12		char in \$v0

Assembly 2 0000000000

General Classes of MIPS Assembly Instructions

- arithmetic operations (+, -, *, /)
- logical operations (&, |, $\tilde{}$, $\hat{}$, «, »)
- data transfer (loads from memory or stores to memory)
- transfers of control (jumps, branches, calls, returns)

Logical operations: MIPS Shift Instructions

- Shift instructions move the bits in a word to the left or right by a specified amount.
- Shifting left (right) by *i* is the same as multiplying (dividing) by 2^{*i*}.
- A logical left (right) shift fills in the vacant bits with zero.
- An arithmetic right shift replicates the most significant bit to fill in the vacant bits.

Example		Meaning	Comment	
sll	\$t2,\$t3,2	\$t2 = \$t3 << 2	shift left logical	
sllv	\$t3,\$t4,\$t5	\$t3 = \$t4 << \$t5	shift left logical variable	
sra	\$t4,\$t3,1	\$t4 = \$t3 >> 1	shift right arithmetic (signed)	
srav	\$t7,\$t2,\$t4	\$t7 = \$t2 >> \$t4	shift right arithmetic variable (signed)	
srl	\$t2,\$t3,7	\$t2 = \$t3 >> 7	shift right logical (unsigned)	
srlv	\$t3,\$t4,\$t6	\$t3 = \$t4 >> \$t6	shift right logical variable (unsigned)	

Exercise: Using Shift Instructions

- Write a single MIPS assembly instruction to multiply \$t2 by 4 (2²) and put the result in \$t3.
- Answer: sll \$t3 \$t2 2.
- Assume \$t1 has the value 2. What are the values assigned to \$t2 if we perform sll \$t2,\$t1,3?
- Answer: shift left by 3 bits > multiply value by 2^3 . The result is $2 \times 2^3 = 16$.
- Assume \$t2 has the value -4. What are the values assigned to \$t3 and \$t4 if we perform the following instructions? sra \$t3,\$t2,2 srl \$t4,\$t2,2

Data Transfer Instructions

- The processors keep only a small amount of data in registers, but memory contains billions of data elements
- Data transfer instructions are used to transfer data between register and memory
- The MIPS can only access memory with load and store instructions.

Specifying Memory Address

- Memory is organized as an array of bytes (8 bits)
- In memory, each element is kept as a word (4 bytes), which must start at address that are multiples of 4.



- How to get the address of a element in the array?
- Base address + offset (multiples of 4)

General Form of MIPS Data Transfer Instructions

- form: <operation> <reg1>,<constant>(<reg2>)
- reg2: keep base address; constant: keep offset
- load instruction: copy data from memory to a register
- store instruction: copy data from a register to memory

	Example	Meaning	Comment
lw	\$t2,8(\$t3)	\$t2 = Mem[\$t3 + 8]	32-bit load
lh	\$t3,0(\$t4)	\$t3 = (Mem[\$t4] ₀) ¹⁶ ## Mem[\$t4]	signed 16-bit load
lhu	\$t8,2(\$t3)	\$t8 = 0 ¹⁶ ## Mem[\$t3 + 2]	unsigned 16-bit load
lb	\$t4,0(\$t5)	\$t4 = (Mem[\$t5] ₀) ²⁴ ## Mem[\$t5]	signed 8-bit load
lbu	\$t6,1(\$t9)	\$t6 = 0 ²⁴ ## Mem[\$t9 + 1]	unsigned 8-bit load
SW	\$t5,-4(\$t2)	$Mem[$t2 - 4] = {}_{32} $t5$	32-bit store
sh	\$t6,12(\$t3)	Mem[\$t3 + 12] = \$t6 ₁₆₃₁	16-bit store
sb	\$t7,1(\$t3)	Mem[\$t3 + 1] = \$t7 ₂₄₃₁	8-bit store

 ##: contatenation; =#: # are assigned; 0[#]: # bits of zero; #1..#2: bit range where the LSB is labeled bit 31.

Indexing Array Elements with a Constant Index

- Use MIPS assembly directives to declare a four element integer array named A.
- Write MIPS assembly instructions to accomplish the following C statement. Assume \$t5, \$t6, and \$t7 are available.

```
A[3] = A[0] + A[1] + A[2]:
.data
_A: .word 1,2,3,0
                        # declare space for array A
.text
. . .
la
     $t5,_A
                 # load address of A
] w
     $t6,0($t5)
                   # load A[0]
lw
     $t7,4($t5)
                   # load A[1]
addu
     $t6,$t6,$t7
                  # add A[0] and A[1]
     $t7.8($t5)
                   # load A[2]
1 พ
addu
     $t6,$t6,$t7
                  # add A[2]
     $t6,12($t5)
                   # store into A[3]
SW
```

Indexing Array Elements with a Variable Index

• Assembly code can be written to access array elements using a variable index. Consider the following source code fragment.

int a[100], i;

... a[i] = a[i] + 1;

• Assume the value of i is in \$t0. The following MIPS code performs this assignment.

.data

```
.space 400
                         # declare space for array _a
a:
. . .
la
     $t1,_a
                   # load address of _a
     $t2,$t0,2
sll
                    # determine offset from _a
     $t2,$t2,$t1
addu
                    # add offset and _a
      $t3,0($t2)
lw
                    # load the value
addiu $t3,$t3,1
                    # add 1 to the value
      $t3.0($t2)
                    # store the value
SW
```

Transfer of Control Instructions

- Transfers of control instructions can cause the next instruction to be executed that is not the next sequential instruction.
- Transfers of control are used to implement control statements in high-level languages.
 - unconditional (goto, break, continue, call, return)
 - conditional (if-then, if-then-else, switch)
 - iterative (while, do, for)

General Form of MIPS Jump and Branch Instructions

- MIPS provides direct jumps to support unconditional transfers of control to a specified location.
- MIPS provides indirect jumps to support returns and switch statements.
- MIPS provides conditional branch instructions to support decision making. MIPS conditional branches test if the values of two registers are equal or not equal.

General Form	Example	Meaning	Comments
j <label></label>	j L1	goto L1;	direct jump
jr <sreg></sreg>	jr \$ra	goto \$ra;	indirect jump
beq <s1reg>,<s2reg>,<label></label></s2reg></s1reg>	beq \$t2,\$t3,L1	if (\$t2 == \$t3) goto L1;	branch equal
bne <s1reg>,<s2reg>,<label></label></s2reg></s1reg>	bne \$t2,\$t3,L1	if (\$t2 != \$t3) goto L1;	branch not equal

• For beq and bne instructions, nothing happens if the condition is not true.

Example of Translating an If Statement

• example source statement:

```
if (i == j)
k = k+i;
```

• Translate into MIPS instructions assuming i, j, and k, are in the registers \$t2, \$t3, and \$t4, respectively.

```
bne $t2,$t3,L1  # if ($t2 != $t3) goto L1
addu $t4,$t4,$t2  # k = k + i
L1:
```

• Note that: the code will be more efficient if we test for the opposite condition to branch over the code that performs the subsequent *then* part of the *if*.

Example of Translating an If-Then-Else Statement

• example source statement:

Exit:

- if (i == j)
 f = g + h;
 else
 f
 - f = g h;
 - Translate into MIPS instructions assuming f, g, h, i, and j are in registers \$s0 through \$s4 respectively.



General Form of MIPS Comparison Instructions

- MIPS provides *set less than* instructions that set a register to 1 if the first source register is less than the value of the second operand. Otherwise it sets it to 0.
- There are versions to perform unsigned comparisons as well.

General Form	Example	Meaning	Comments
slt <dreg>,<s1reg>,<s2reg></s2reg></s1reg></dreg>	slt \$t2,\$t3,\$t4	if (\$t3 < \$t4) \$t2 = 1; else \$t2 = 0;	compare less than
sltu <dreg>,<s1reg>,<s2reg></s2reg></s1reg></dreg>	sltu \$t2,\$t3,\$t4	if (\$t3 < \$t4) \$t2 = 1; else \$t2 = 0;	compare less than unsigned
slti <dreg>,<sreg>,<const></const></sreg></dreg>	slti \$t2,\$t3,100	if (\$t3 < 100) \$t2 = 1; else \$t2 = 0;	compare less than constant
sltiu <dreg>,<s1reg>,<const></const></s1reg></dreg>	sltiu \$t2,\$t3,100	if (\$t3 < 100) \$t2 = 1; else \$t2 = 0;	compare less than constant unsigned

Example of Translating an If-Then-Else Statement

• example source statement:

```
if (a < b)
c = a;
else
```

```
c = b;
```

• Translate into MIPS instructions assuming a, b, and c, are in the registers \$t2, \$t3, and \$t4, respectively. Assume \$t5 is available.

```
slt $t5,$t2,$t3  # a < b
beq $t5,$zero,L1  # if ($t5 == 0) goto L1
move $t4,$t2  # c = a
j  L2  # goto L2
L1:
move $t4,$t3  # c = b
L2:</pre>
```

Translating an If-Statement with a Different Condition

- example source statement:
- if (a > b)
- c = a;
 - Translate into MIPS instructions assuming a, b, and c, are in the registers \$t2, \$t3, and \$t4, respectively. Assume \$t5 is available.

```
slt $t5,$t3,$t2  # b < a
beq $t5,$zero,L1  # if ($t5 == 0) goto L1
or $t4,$t2,$zero  # c = a
L1:</pre>
```

How about the translation for the following statement?
 if (a > = b)
 c = a;

Translating an If-Statement with a Different Condition

- example source statement:
- if (a > = b) c = a:
 - Key point: $a \ge b$ is the same as !(a < b).
 - Translate into MIPS instructions assuming a, b, and c, are in the registers \$t2, \$t3, and \$t4, respectively. Assume \$t5 is available.

slt \$t5,\$t2,\$t3 # a < b
bne \$t5,\$zero,L1 # if (\$t5 != 0) goto L1
or \$t4,\$t2,\$zero # c = a
L1:</pre>

Translating Other High-Level Control Statements

- How can we translate other high-level control statements (while, do, for)?
- We can first express the C statement using C if and goto statements.
- After that we can translate using MIPS unconditional jumps (j), comparisons (slt, slti), and conditional branches (beq, bne).

Assembly 2 0000000000

Example of Translating a For Statement

• example source statement:

```
sum = 0;
for (i = 0; i < 100; i++)
sum += a[i];
```

• First, we replace the for statement using an if and goto statements.

```
sum = 0;
i = 0;
goto test;
loop: sum += a[i];
i++;
test: if (i < 100) goto loop;</pre>
```

Example of Translating a For Statement (cont.)

- We can next translate into MIPS instructions.
- Assume sum, i, and the starting address of a, are in \$t2, \$t3, and \$t4, respectively and that \$t5 is available.

\$t2,0	#	sum = 0
\$t3,\$zero	#	i = 0
test	#	goto test
\$t5,\$t3,2	#	tmp = i*4
\$t5,\$t5,\$t4	#	tmp = tmp + &a
\$t5,0(\$t5)	#	<pre>load a[i] into tmp</pre>
\$t2,\$t2,\$t5	#	sum += tmp
\$t3,\$t3,1	#	i++
\$t5,\$t3,100	#	test i < 100
<pre>\$t5,\$zero,loop</pre>	#	if true goto loop
	<pre>\$t2,0 \$t3,\$zero test \$t5,\$t3,2 \$t5,\$t5,\$t4 \$t5,0(\$t5) \$t2,\$t2,\$t5 \$t3,\$t3,1 \$t5,\$t3,100 \$t5,\$zero,loop</pre>	<pre>\$t2,0 # \$t3,\$zero # test # \$t5,\$t3,2 # \$t5,\$t5,\$t4 # \$t5,0(\$t5) # \$t2,\$t2,\$t5 # \$t3,\$t3,1 # \$t5,\$t3,100 # \$t5,\$zero,loop #</pre>

Optimizing the Translation of the For Statement

```
sum = 0;
for (i = 0; i < 100; i++)
    sum += a[i];
```

- How can we make the code on the previous two slides more efficient?
 - We don't need to test the exit condition the first time.
 - We can step through the array since each element is 4 bytes after the last element.
 - We can efficiently check if we have stepped past the last element to be processed.

```
sum = 0;
i = 0;
goto test;
loop: sum += a[i];
i++;
test: if (i < 100) goto loop;</pre>
sum = 0;
p = &a;
exit = &a[100];
loop: sum += *p;
p++;
if (p != exit) goto loop;
```

Optimizing the Translation of the For Statement (cont.)

- Again assume sum and the starting address of a are in \$t2 and \$t4, respectively. Also assume that \$t3 and \$t5 are available.
- We can reduce the body of the loop from 7 instructions to 4 instructions.

```
and
     $t2.$t2.$zero
                       \# sum = 0
     $t3.$t4
                      \# p = \&a
move
addiu $t5,$t3,400
                      # exit = &a[100]
loop:
lw
     $t6,0($t3)
                       # load a[i] into tmp
addu $t2,$t2,$t6
                       # sum += tmp
addiu $t3,$t3,4
                       # p++
      $t3,$t5,loop
                       # if (p != exit) goto loop
bne
```

Steps for Executing a Function

• caller actions for the function call

- Place arguments where the callee can access them: a0 a3
- Place return address where the callee can access it.
- Transfer control to the callee: jal LI (Li is the label of the callee)
- callee actions when entering function
 - Allocating storage needed for the callee: \$s0 \$s7, \$t0 \$t9
 - Preserve values of callee-save registers used in the function: \$s0 - \$s7
 - addi \$sp, \$sp, -4
 - sw \$0, 0(\$sp)
- callee performs the task associated with the function

Steps for Executing a Function (cont.)

- callee actions when exiting function:
 - Assign the result value in a place where caller can access it: v0- v1,
 - Restore the values of callee-save registers used in the function.
 - lw \$s0, 0(\$sp)
 - addi \$sp, \$sp, 4
 - Deallocate storage needed for the callee.
 - Transfers control back to the point after the call: jr \$ra
- caller accesses the result value

MIPS Instruction Formats

- R format is used for shifts and instructions that reference only registers.
- I format is used for loads, stores, branches, and immediate instructions.
- J format is used for jump and call instructions.

Name		Fields				
Field Size	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits
R format	ор	rs	rt	rd	shamt	funct
I format	ор	rs rt immed				
J format	op	targaddr				

op - instruction opcodeshamt - shift amountrs - first register source operandfunct - additional opcodesrt - second register source operandimmed - offsets/constantsrd - register destination operandtargaddr - jump/call target

MIPS R Format

- The MIPS R format is used for instructions that only reference registers and for shift operations.
- The op field must have the value of zero for the R format to be used.
- The funct field indicates the type of operation to be performed for R format instructions.
- The shamt field is only used for the sll, sra, and srl instructions since the shift amount for words cannot exceed the unsigned value 31 (5 bits) and there were more available opcode values in the funct field than the op field.

Name		Fields				
Field Size	6 bits	6 bits 5 bits 5 bits 5 bits 6 bits				
R format	op	rs	rt	rd	shamt	funct

- op instruction opcode
- rs first register source operand
- rt second register source operand

rd – register destination operand shamt – shift amount funct – additional opcodes

R Format Instruction Encoding Examples

• R-format example 1: addu \$t2,\$t3,\$t4

fields	op	rs	rt	rd	shamt	funct	
size	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	
decimal	0	11	12	10	0	33	
binary	000000	000000 01011 01100 01010 00000 100001					
hexadecimal	0x016c5021						

• R-format example 2: sll \$t5,\$t6,7

fields	op	rs	rt	rd	shamt	funct	
size	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	
decimal	0	0	14	13	7	0	
binary	000000	000000 00000 01110 01101 00111 000000					
hexadecimal	0x000e69c0						

MIPS I Format

- The MIPS I format is used for arithmetic/logical immediate instructions, loads and stores, and conditional branches.
- The op field is used to identify the type of instruction.
- The rs field is used as a source register.
- The rt field is used as a source or destination register, depending on the instruction.
- The immed field is sign extended if it is an arithmetic operation. It is zero extended if it is a logical operation.

Name	Fields				
Field Size	6 bits	5 bits	5 bits	16 bits	
I format	op	rs	rt	immed	

op – instruction opcode rs – first register source operand rt – second register source operand immed – offsets/constants

Assembly 2 00000000000

I Format Instruction Encoding Examples

• I-format example 1: addiu \$t0,\$t0,1

fields	op	rs	rt	immed			
size	6 bits	5 bits	5 bits	16 bits			
decimal	9	8	8	1			
binary	001001	001001 01000 01000 00000000000000000000					
hexadecimal	0x25080001						

• I-format example 2: lw \$s1,100(\$s2)

fields	op	rs	rt	immed			
size	6 bits	5 bits	5 bits	16 bits			
decimal	35	18	17	100			
binary	100011	100011 10010 10001 00000000110010					
hexadecimal	0x8e510064						

I Format Instruction Encoding Examples (cont.)

- Conditional branches are also encoded using the I format.
- The branch displacement is a signed value in instructions (not bytes) from the point of the branch.
- branch example:
- L2: instruction
- instruction
- instruction

beq \$t6,\$t7,L2

fields	op	rs	rt	immed			
size	6 bits	5 bits	5 bits	16 bits			
decimal	4	14	15	-3			
binary	000100	000100 01110 01111 1111111111111					
hexadecimal	0x11cffffd						

Number Representation

Assembly 2 000000000000

Branch Example of MIPS I Format (cont.)

address	instruction
4000008	addi \$5, \$5, 1
400000C	beq \$0, \$5, label
40000010	addi \$5, \$5, 1
40000014	addi \$5, \$5, 1
40000018	label addi \$5, \$5, 1
4000001C	addi \$5, \$5, 1
40000020	etc

- Binary code to beq \$0,\$5, label is 0x10050002, which means 2 instructions from the next instruction.
- Before executing beq: PC = 0x4000000C
- After executing beq: $PC+4 = 0 \times 40000010$
- Relative address 4*2 = 0x0000008
- Effective Address = 0x40000018

ор	rs	rt	Immediate value
00010	00000	00101	000000000000000000000000000000000000000

MIPS J Format

- The MIPS J format is used for unconditional jumps and function calls.
- The op field is used to identify the type of instruction.
- The targaddr field is used to indicate an absolute target instruction address divided by 4.
 - An absolute target instruction address divided by 4 means shift its binary representations 2 bits to the right.

Name	Fields	
Field Size	6 bits	26 bits
J format	op	targaddr

op - instruction opcode

targaddr - jump/call target

Example of MIPS J Format

