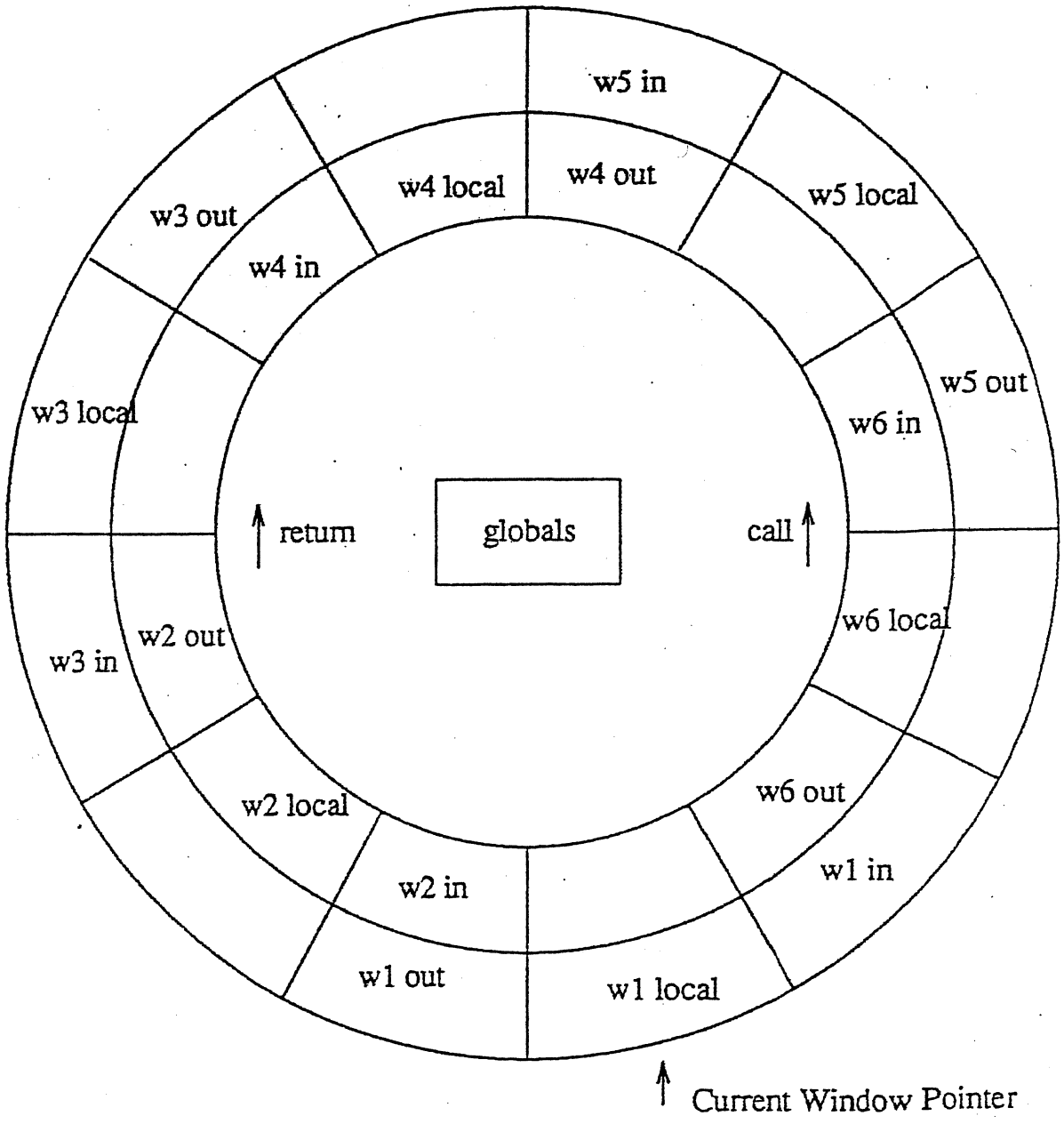
Figure 2-2 *Overlapping Register Windows*



2

Instruction-set Mapping

The tables in this chapter describe the relationship between hardware instructions of the SPARC architecture, as defined in *SPARC Processor Architecture*, and the instruction set used by Sun Microsystems' SPARC Assembler.

2.1. Table Notation

The following table describes the notation used in the tables in the rest of the chapter to describe the instruction set of the assembler. In the table below, the vertical bar | indicates alternation, but brackets [ ] are to be taken literally:

Table 2-1 *Notation*

Symbol	*Describes*	*Comment*

reg	`%0 ... %31`
	`%g0 ... %g7`
	`%o0 ... %o7`
	`%l0 ... %l7`
	`%i0 ... %i7`
		
		(same as `%0...%7`*)*
		(same as `%8...%15`*)*
		(same as `%16...%23`*)*
		(same as `%24...%31`*)*

freg	`%f0 ... %f31`	
creg	`%c0 ... %c31`	
value		*(an expression involving at most one relocatable symbol)*
const13	*value*	*(a signed constant which fits in 13 bits)*
const22	*value*	*(a constant which fits in 22 bits)*
asi	*value*	*(alternate address space identifier; an unsigned value fitting in 8 bits)*
reg_{rd}		*Destination register.*
reg_{rs1}, reg_{rs2}		*Source register 1, source register 2.*
regaddr		*Address formed with register contents only.*
address	reg_{rs1} + reg_{rs2} reg_{rs1} + *const13* reg_{rs1} − *const13* *const13* + reg_{rs1} *const13*	*Address formed from register contents, immediate constant, or both.*

Table 2-1 Notation— Continued

Symbol	*Describes*	*Comment*
reg_or_imm	reg_{rs2} *const13*	*Value from either a single register, or an immediate constant.*

2.2. Hardware Integer Instructions

The following table outlines the correspondence between SPARC hardware instructions and SPARC assembly-language instructions. The following notations are suffixed repeatedly to assembler mnemonics (and in upper case for SPARC architecture instruction names):

sr — for status register.

a — for instructions dealing with alternate space.

b — for byte instructions.

h — for halfword instructions.

d — for double-word instructions.

f — for referencing floating-point registers.

c — for referencing coprocessor registers.

rd — as a subscript, refers to a destination register in the argument list of an instruction.

rs — as a subscript, refers to a source register in the argument list of an instruction.

NOTE *The syntax of individual instructions is designed so that a destination operand (if any), which may be either a register or a reference to a memory location, is always the last operand in a statement.*

NOTE *All* `Bicc` *and* `Bfcc` *instructions, described in the following table, may indicate that the* annul *bit is to be set by appending* "`,a`" *to the opcode; e.g.* "`bgeu,a` *label*". The following syntax descriptions indicate the optional "`,a`" *by enclosing it in* { }*:*

Table 2-2 *SPARC to Assembly Language Mapping*

SPARC	*Mnemonic*	*Argument List*	*Name*	*Comments*
LDSB	`ldsb`	[*address*], reg_{rd}	*Load signed byte.*	
LDSH	`ldsh`	[*address*], reg_{rd}	*Load signed halfword.*	
LDUB	`ldub`	[*address*], reg_{rd}	*Load unsigned byte.*	
LDUH	`lduh`	[*address*], reg_{rd}	*Load unsigned halfword.*	
LD	`ld`	[*address*], reg_{rd}	*Load word.*	
D	`ldd`	[*address*], reg_{rd}	*Load double word.*	(reg_{rd} *must be even*)

Table 2-2 *SPARC to Assembly Language Mapping— Continued*

SPARC	*Mnemonic*	*Argument List*	*Name*	*Comments*
LDF	`ld`	[*address*], *freg*$_{rd}$	*Load floating-point register.*	
LDFSR	`ld`	[*address*], `%fsr`		
LDDF	`ldd`	[*address*], *freg*$_{rd}$	*Load double floating-point.*	
LDC	`ld`	[*address*], *creg*$_{rd}$	*Load coprocessor.*	
LDCSR	`ld`	[*address*], `%csr`		
LDDC	`ldd`	[*address*], *creg*$_{rd}$	*Load double coprocessor.*	
LDSBA	`ldsba`	[*regaddr*] *asi*, *reg*$_{rd}$	*Load signed byte from alternate space.*	
LDSHA	`ldsha`	[*regaddr*] *asi*, *reg*$_{rd}$		
LDUBA	`lduba`	[*regaddr*] *asi*, *reg*$_{rd}$		
LDUHA	`lduha`	[*regaddr*] *asi*, *reg*$_{rd}$		
LDA	`lda`	[*regaddr*] *asi*, *reg*$_{rd}$		
LDDA	`ldda`	[*regaddr*] *asi*, *reg*$_{rd}$		(*reg*$_{rd}$ *must be even)*
STB	`stb`	*regaddr*, [*address*]	*Store byte.*	(*synonyms:* `stub`, `stsb`)
STH	`sth`	*regaddr*, [*address*]		(*synonyms:* `stuh`, `stsh`)
ST	`st`	*reg*$_{rd}$, [*address*]		
STD	`std`	*reg*$_{rd}$, [*address*]		(*reg*$_{rd}$ *must be even)*
STF	`st`	*freg*$_{rd}$, [*address*]		
STDF	`std`	*freg*$_{rd}$, [*address*]		
STFSR	`st`	`%fsr`, [*address*]	*Store floating-point status register.*	
STDFQ	`std`	`%fq`, [*address*]	*Store double floating-point queue.*	
STC	`st`	*creg*$_{rd}$, [*address*]	*Store coprocessor.*	
STDC	`std`	*creg*$_{rd}$, [*address*]		
STCSR	`st`	`%csr`, [*address*]		
STDCQ	`std`	`%cq`, [*address*]	*Store double coprocessor queue.*	
STBA	`stba`	*regaddr*, [*regaddr*] *asi*	*Store byte into alternate space.*	(*synonyms:* `stuba`, `stsba`)
STHA	`stha`	*regaddr*, [*regaddr*] *asi*		(*synonyms:* `stuha`, `stsha`)
STA	`sta`	*reg*$_{rd}$, [*regaddr*] *asi*		
STDA	`stda`	*reg*$_{rd}$, [*regaddr*] *asi*		(*reg*$_{rd}$ *must be even)*
LDSTUB	`ldstub`	[*address*], *reg*$_{rd}$	*Load-store unsigned byte.*	
LDSTUBA	`ldstuba`	[*regaddr*] *asi*, *reg*$_{rd}$		
SWAP	`swap`	[*address*], *reg*$_{rd}$	*Swap memory word with register.*	
SWAPA	`swapa`	[*regaddr*] *asi*, *reg*$_{rd}$		

Table 2-2 *SPARC to Assembly Language Mapping— Continued*

SPARC	*Mnemonic*	*Argument List*	*Name*	*Comments*

ADD
ADDcc
ADDX
ADDXcc
	`add`
	`addcc`
	`addx`
	`addxcc`
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
			Add
			Add and modify icc.
			Add with carry.	

SUB
SUBcc
SUBX
SUBXcc
	`sub`
	`subcc`
	`subx`
	`subxcc`
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
			Subtract.
			Subtract and modify icc.
			Subtract with carry.	

MULScc	`mulscc`	reg_{rs2}, *reg_or_imm*, reg_{rd}	*Multiply step (and modify icc).*	

AND
ANDcc
ANDN
ANDNcc
OR
ORcc
ORN
ORNcc
	`and`
	`andcc`
	`andn`
	`andncc`
	`or`
	`orcc`
	`orn`
	`orncc`
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
			And.
			
			Inclusive or.	

XOR XORcc	`xor` `xorcc`	reg_{rs2}, *reg_or_imm*, reg_{rd} reg_{rs2}, *reg_or_imm*, reg_{rd}	*Exclusive or.*	
XNOR XNORcc	`xnor` `xnorcc`	reg_{rs2}, *reg_or_imm*, reg_{rd} reg_{rs2}, *reg_or_imm*, reg_{rd}	*Exclusive nor.*	

TADDcc
TSUBcc
TADDccTV
 	
TSUBccTV
	`taddcc`
	`tsubcc`
	`taddcctv`
	
	`tsubcctv`
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		
		reg_{rs2}, *reg_or_imm*, reg_{rd}
			Tagged add.
			
			Tagged add and modify icc and trap on overflow.	

SLL
SRL
SRA
	`sll`
	`srl`
	`sra`
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
		reg_{rs2}, *reg_or_imm*, reg_{rd}
			Shift left logical.
			Shift right logical.
			Shift right arithmetic.	

SETHI	`sethi` `sethi`	*const22*, reg_{rd} `%hi(`*value*`)`, reg_{rd}	*Set high 22 bits of r register.*	 *(see pseudo-instructions)*
SAVE RESTORE	`save` `restore`	reg_{rs1}, *reg_or_imm*, reg_{rd} reg_{rs1}, *reg_or_imm*, reg_{rd}		*(see pseudo-instructions)* *(see pseudo-instructions)*

Bicc	`bn{,a}`
	
	`bne{,a}`
	`be{,a}`
	`bg{,a}`
		label
		
		label
		label
		label
			Branch on integer condition codes..	*(branch never)*
				
				(synonym: `bnz`*)*
				(synonym: `bz`*)*

Table 2-2 *SPARC to Assembly Language Mapping— Continued*

SPARC	*Mnemonic*	*Argument List*	*Name*	*Comments*
Bicc	`ble{,a}`	*label*		
	`bge{,a}`	*label*		
	`bl{,a}`	*label*		
	`bgu{,a}`	*label*		
	`bleu{,a}`	*label*		
	`bcc{,a}`	*label*		*(synonym:* `bgeu`*)*
	`bcs{,a}`	*label*		*(synonym:* `blu`*)*
	`bpos{,a}`	*label*		
	`bneg{,a}`	*label*		
	`bvc{,a}`	*label*		
	`bvs{,a}`	*label*		
	`ba{,a}`	*label*		*(synonym:* `b`*)*
FBfcc	`fbn{,a}`	*label*	*Branch on floating-point condition codes.*	*(branch never)*
	`fbu{,a}`	*label*		
	`fbg{,a}`	*label*		
	`fbug{,a}`	*label*		
	`fbl{,a}`	*label*		
	`fbul{,a}`	*label*		
	`fblg{,a}`	*label*		
	`fbne{,a}`	*label*		*(synonym:* `fbnz`*)*
	`fbe{,a}`	*label*		*(synonym:* `fbz`*)*
	`fbue{,a}`	*label*		
	`fbge{,a}`	*label*		
	`fbuge{,a}`	*label*		
	`fble{,a}`	*label*		
	`fbule{,a}`	*label*		
	`fbo{,a}`	*label*		
	`fba{,a}`	*label*		
CBccc	`cbn{,a}`	*label*	*Branch on coprocessor condition codes.*	*(branch never)*
	`cb3{,a}`	*label*		
	`cb2{,a}`	*label*		
	`cb23{,a}`	*label*		
	`cb1{,a}`	*label*		
	`cb13{,a}`	*label*		
	`cb12{,a}`	*label*		
	`cb123{,a}`	*label*		
	`cb0{,a}`	*label*		
	`cb03{,a}`	*label*		
	`cb02{,a}`	*label*		
	`cb023{,a}`	*label*		
	`cb01{,a}`	*label*		
	`cb013{,a}`	*label*		
	`cb012{,a}`	*label*		
	`cba{,a}`	*label*		

Table 2-2 *SPARC to Assembly Language Mapping—Continued*

SPARC	*Mnemonic*	*Argument List*	*Name*	*Comments*
CALL	`call`	*label*`[,`*n*`]`	*(n = # of out registers used as arguments)*	
UNIMP	`unimp`	*const22*	*Unimplemented instruction.*	
JMPL	`jmpl`	*address*, reg_{rd}	*Jump and link.*	
RETT	`rett`	*address*	*Return from trap.*	
IFLUSH	`iflush`	*address*	*Instruction cache flush.*	
Ticc	`tn`	*address*	*Trap on integer condition code. (See note.)*	*(trap never)*
	`tne`	*address*		*(synonym:* `tnz`*)*
	`te`	*address*		*(synonym:* `tz`*)*
	`tg`	*address*		
	`tle`	*address*		
	`tge`	*address*		
	`tl`	*address*		
	`tgu`	*address*		
	`tleu`	*address*		
	`tlu`	*address*		*(synonym:* `tcc`*)*
	`tgeu`	*address*		*(synonym:* `tcs`*)*
	`tpos`	*address*		
	`tneg`	*address*		
	`tvc`	*address*		
	`tvs`	*address*		
	`ta`	*address*		*(synonym:* `t`*)*
RDY	`rd`	`%y`, reg_{rd}		*(see pseudo-instructions)*
RDPSR	`rd`	`%psr`, reg_{rd}		*(see pseudo-instructions)*
RDWIM	`rd`	`%wim`, reg_{rd}		*(see pseudo-instructions)*
RDTBR	`rd`	`%tbr`, reg_{rd}		*(see pseudo-instructions)*
WRY	`wr`	reg_{rs1}, *reg_or_imm*, `%y`		*(see pseudo-instructions)*
WRPSR	`wr`	reg_{rs1}, *reg_or_imm*, `%psr`		*(see pseudo-instructions)*
WRWIM	`wr`	reg_{rs1}, *reg_or_imm*, `%wim`		*(see pseudo-instructions)*
WRTBR	`wr`	reg_{rs1}, *reg_or_imm*, `%tbr`		*(see pseudo-instructions)*

NOTE *Trap numbers 16-31 are available for use by the user, and will not be usurped by Sun. Currently-defined trap numbers are those defined in* `/usr/include/sun4/trap.h`, *as follows:*

```
0x00  ST_SYSCALL
0x01  ST_BREAKPOINT
0x02  ST_DIV0
0x03  ST_FLUSH_WINDOWS
```

```
0x04  ST_CLEAN_WINDOWS
0x05  ST_RANGE_CHECK
```

2.3. Hardware Floating-Point Instructions

In the table below, the types of numbers being manipulated by an instruction are denoted by the following lowercase letters:

i — integer

s — single

d — double

x — extended

In some cases where more than numeric type is involved, each instruction in a group is described. Otherwise, only the first member of a group is described.

Table 2-3 *Floating-point Instructions*

SPARC	*Mnemonic*	*Argument List*	*Description*
FiTOs	fitos	$freg_{rs2}$, $freg_{rd}$	*Convert integer to single.*
FiTOd	fitod	$freg_{rs2}$, $freg_{rd}$	*Convert integer to double.*
FiTOx	fitox	$freg_{rs2}$, $freg_{rd}$	*Convert integer to extended.*
FsTOi	fstoi	$freg_{rs2}$, $freg_{rd}$	*Convert single to integer.*
FdTOi	fdtoi	$freg_{rs2}$, $freg_{rd}$	*Convert double to integer.*
FxTOi	fxtoi	$freg_{rs2}$, $freg_{rd}$	*Convert extended to integer.*
FINTs	fints	$freg_{rs2}$, $freg_{rd}$	*Convert to integral-valued single.*
FINTd	fintd	$freg_{rs2}$, $freg_{rd}$	*Convert to integral-valued double.*
FINTx	fintx	$freg_{rs2}$, $freg_{rd}$	*Convert to integral-valued extended.*
FINTRZs	fintrzs	$freg_{rs2}$, $freg_{rd}$	*Convert to integral-valued single & round toward zero.*
FINTRZd	fintrzd	$freg_{rs2}$, $freg_{rd}$	*Convert to integral-valued double & round toward zero.*
FINTRZx	fintrzx	$freg_{rs2}$, $freg_{rd}$	*Convert to integral-valued extended & round toward zero.*
FsTOd	fstod	$freg_{rs2}$, $freg_{rd}$	*Convert single to double.*
FsTOx	fstox	$freg_{rs2}$, $freg_{rd}$	*Convert single to extended.*
FdTOs	fdtos	$freg_{rs2}$, $freg_{rd}$	*Convert double to single.*
FdTOx	fdtox	$freg_{rs2}$, $freg_{rd}$	*Convert double to extended.*
FxTOd	fxtod	$freg_{rs2}$, $freg_{rd}$	*Convert extended to double.*
FxTOs	fxtos	$freg_{rs2}$, $freg_{rd}$	*Convert extended to single.*
FMOVs	fmovs	$freg_{rs2}$, $freg_{rd}$	*move*
FNEGs	fnegs	$freg_{rs2}$, $freg_{rd}$	*negate*
FABSs	fabss	$freg_{rs2}$, $freg_{rd}$	*absolute value*
FCLASSs	fclasss	$freg_{rs2}$, $freg_{rd}$	*classify*
FCLASSd	fclassd	$freg_{rs2}$, $freg_{rd}$	

Table 2-3 *Floating-point Instructions— Continued*

SPARC	*Mnemonic*	*Argument List*	*Description*
FCLASSx	fclassx	$freg_{rs2}$, $freg_{rd}$	
FEXPOs	fexpos	$freg_{rs2}$, $freg_{rd}$	*extract exponent*
FEXPOd	fexpod	$freg_{rs2}$, $freg_{rd}$	
FEXPOx	fexpox	$freg_{rs2}$, $freg_{rd}$	
FSQRTs	fsqrts	$freg_{rs2}$, $freg_{rd}$	*square root*
FSQRTd	fsqrtd	$freg_{rs2}$, $freg_{rd}$	
FSQRTx	fsqrtx	$freg_{rs2}$, $freg_{rd}$	
FADDs	fadds	$freg_{rs1}$, $freg_{rs2}$, $freg_{rd}$	*add*
FADDd	faddd	$freg_{rs1}$, $freg_{rs2}$, $freg_{rd}$	
FADDx	faddx	$freg_{rs1}$, $freg_{rs2}$, $freg_{rd}$	
FSUBs	fsubs	$freg_{rs1}$, $freg_{rs2}$, $freg_{rd}$	*subtract*
FSUBd	fsubd	$freg_{rs1}$, $freg_{rs2}$, $freg_{rd}$	
FSUBx	fsubx	$freg_{rs1}$, $freg_{rs2}$, $freg_{rd}$	
FMULs	fmuls	$freg_{rs1}$, $freg_{rs2}$, $freg_{rd}$	*multiply*
FMULd	fmuld	$freg_{rs1}$, $freg_{rs2}$, $freg_{rd}$	
FMULx	fmulx	$freg_{rs1}$, $freg_{rs2}$, $freg_{rd}$	
FDIVs	fdivs	$freg_{rs1}$, $freg_{rs2}$, $freg_{rd}$	*divide*
FDIVd	fdivd	$freg_{rs1}$, $freg_{rs2}$, $freg_{rd}$	
FDIVx	fdivx	$freg_{rs1}$, $freg_{rs2}$, $freg_{rd}$	
FSCALEs	fscales	$freg_{rs2}$, $freg_{rd}$	*scale*
FSCALEd	fscaled	$freg_{rs2}$, $freg_{rd}$	
FSCALEx	fscalex	$freg_{rs2}$, $freg_{rd}$	
FREMs	frems	$freg_{rs2}$, $freg_{rd}$	*partial remainder*
FREMd	fremd	$freg_{rs2}$, $freg_{rd}$	
FREMx	fremx	$freg_{rs2}$, $freg_{rd}$	
FQUOTs	fquots	$freg_{rs2}$, $freg_{rd}$	*partial quotient*
FQUOTd	fquotd	$freg_{rs2}$, $freg_{rd}$	
FQUOTx	fquotx	$freg_{rs2}$, $freg_{rd}$	
FCMPs	fcmps	$freg_{rs1}$, $freg_{rs2}$	*compare*
FCMPd	fcmpd	$freg_{rs1}$, $freg_{rs2}$	
FCMPx	fcmpx	$freg_{rs1}$, $freg_{rs2}$	
FCMPEs	fcmpes	$freg_{rs1}$, $freg_{rs2}$	*Compare, generate exception if unordered.*
FCMPEd	fcmped	$freg_{rs1}$, $freg_{rs2}$	
FCMPEx	fcmpex	$freg_{rs1}$, $freg_{rs2}$	

2.4. Pseudo-Instructions

This section describes the mapping of pseudo-instructions to hardware instructions.

Table 2-4 *Pseudo-Instruction to Hardware Instruction Mapping*

Pseudo-Instruction	*Hardware Equivalent(s)*	*Comment*
`nop`	`sethi 0, %g0`	*(no-op)*
`cmp` reg_{rs1}, *reg_or_imm*	`subcc` reg_{rs1}, *reg_or_imm*, `%g0`	*(compare)*
`jmp` *address*	`jmpl` *address*, `%g0`	
`call` *reg_or_imm*	`jmpl` *reg_or_imm*, `%o7`	
`tst` reg_{rs1}	`orcc` reg_{rs1}, `%g0, %g0`	*(test)*
`ret`	`jmpl %i7+8, %g0`	*(return from subroutine)*
`retl`	`jmpl %o7+8, %g0`	*(return from leaf subroutine)*
`restore`	`restore %g0, %g0, %g0`	*(trivial* `restore`*)*
`save`	`save %g0, %g0, %g0`	*(trivial* `save`*)* *Warning: trivial* `save` *should only be used in kernel code!*
`set` *value*, reg_{rd}	`or %g0,` *value*, reg_{rd}	*(if -4096 ≤ value ≤ 4095)*
`set` *value*, reg_{rd}	`sethi %hi(`*value*`),` reg_{rd}	*(if ((value&0x1ff) == 0))*
`set` *value*, reg_{rd}	`sethi %hi(`*value*`),` reg_{rd} `; or` reg_{rd}`, %lo(`*value*`),` reg_{rd}	*(otherwise)* *Warning: do not use* `set` *in an instruction's delay slot.*
`not` reg_{rs1}, reg_{rd}	`xnor` reg_{rs1}, `%g0,` reg_{rd}	*(one's complement)*
`not` reg_{rd}	`xnor` reg_{rd}, `%g0,` reg_{rd}	*(one's complement)*
`neg` reg_{rs2}, reg_{rd}	`sub %g0,` reg_{rs2}, reg_{rd}	*(two's complement)*
`neg` reg_{rd}	`sub %g0,` reg_{rd}, reg_{rd}	*(two's complement)*
`inc` reg_{rd}	`add` reg_{rd}, `1,` reg_{rd}	*(increment by 1)*
`inc` *const13*, reg_{rd}	`add` reg_{rd}, *const13*, reg_{rd}	*(increment by const13)*
`inccc` reg_{rd}	`addcc` reg_{rd}, `1,` reg_{rd}	*(increment by 1 and set icc)*
`inccc` *const13*, reg_{rd}	`addcc` reg_{rd}, *const13*, reg_{rd}	*(increment by const13 and set icc)*
`dec` reg_{rd}	`sub` reg_{rd}, `1,` reg_{rd}	*(decrement by 1)*
`dec` *const13*, reg_{rd}	`sub` reg_{rd}, *const13*, reg_{rd}	*(decrement by const13)*
`deccc` reg_{rd}	`subcc` reg_{rd}, `1,` reg_{rd}	*(decrement by 1 and set icc)*
`deccc` *const13*, reg_{rd}	`subcc` reg_{rd}, *const13*, reg_{rd}	*(decrement by const13 and set icc)*