CDA3101 Exam 2 Study Topics

Covers slides, assignments 4-5, examples presented in class, and sections 4.5-4.10, 4.14, 6.1-6.7, 6.14 from the textbook.

1. Multicycle Portion of MIPS Design Slide Set
    1.1. Steps for Multicycle Operations
    1.2. Multicycle Datapath
    1.3. Multicycle Control
        1.3.1. Control Signals
        1.3.2. Finite State Machine Implementation

2. Pipeline 1 Slide Set
    2.1. Pipeline Introduction
        2.1.1. Pipeline Speedup
        2.1.2. Pipeline Terms
        2.1.3. Pipeline Diagrams
    2.2. Hazards
        2.2.1. Structural Hazards
        2.2.2. Data Hazards
            2.2.2.1. Dependences
            2.2.2.2. Forwarding
            2.2.2.3. Stalls
            2.2.2.4. Instruction Scheduling
        2.2.3. Control Hazards
            2.2.3.1. Control Dependences
            2.2.3.2. Predicting Not Taken
            2.2.3.3. Branch Prediction by the Compiler
    2.3. Pipeline Datapath
        2.3.1. Pipeline Registers
    2.4. Pipeline Control
        2.4.1. Control Signals
            2.4.1.1. Control for Forwarding
            2.4.1.2. Control for Stalling
        2.4.2. Reducing the Delay of Branches
            2.4.2.1. Resolving Branch in ID Stage
            2.4.2.2. 1-Bit Branch Prediction Buffer
            2.4.2.3. 2-Bit Branch Prediction Buffer
            2.4.2.4. Branch Target Buffer
            2.4.2.5. Delayed Branches

3. Pipeline 2 Slide Set
    3.1. Exceptions
        3.1.1. Multiple Exceptions
        3.1.2. Precise Exceptions
    3.2. Multicycle Operations
        3.2.1. Complications Due to Multicycle Operations
    3.3. More ILP
        3.3.1. Superpipelining
        3.3.2. Static Multiple Issue
            3.3.2.1. Loop Unrolling
            3.3.2.2. Scheduling Instructions
        3.3.3. Dynamic Multiple Issue
        3.3.4. Out-of-Order Execution

4. Parallel Slide Set
    4.1. Multiprocessor Introduction
        4.1.1. Multiprocessor Definitions
        4.1.2. Trend toward Multiprocessing
        4.1.3. Challenges of Creating Parallel Programs
        4.1.4. Levels of Parallelism
        4.1.5. Categorizing Hardware for Parallelism
    4.2. SIMD Processors
        4.2.1. Vector Processors
        4.2.2. SIMD Extensions to GP Processors
    4.3. Multithreading
    4.4. Shared Memory Multiprocessors
    4.5. GPUs
    4.6. Message Passing Multiprocessors
    4.7. Warehouse-Scale Computers