CDA3101 Exam 1 Study Topics

Covers slides, assignments 1-3, examples presented in class, and sections 1.1-1.4, 1.6-1.8, 2.2-2.3, 2.5-2.7, 2.10, 2.12, 4.1-4.4, A.9, B.2-B.3, B.7-B.10 from the textbook.

1. Introduction Slide Set
    - 1.1. Classes of Computers
    - 1.2. Great Architecture Ideas
    - 1.3. Software Levels
    - 1.4. Hardware Parts
    - 1.5. Measures
        - 1.5.1. Latency vs Bandwidth
        - 1.5.2. Performance vs Execution Time
        - 1.5.3. N Times Faster
        - 1.5.4. Clock Periods and Clock Rates
        - 1.5.5. Data Sizes
        - 1.5.6. CPU Time
        - 1.5.7. Amdahl's Law
    - 1.6. Hardware Trends

2. Assembly Slide Set
    - 2.1. MIPS Introduction
    - 2.2. Encoding
    - 2.3. MIPS Addressing Modes
    - 2.4. MIPS Instruction Formats
        - 2.4.1. R Format
        - 2.4.2. I Format
        - 2.4.3. J Format
    - 2.5. Arithmetic Operations
        - 2.5.1. Adds and Subtracts
        - 2.5.2. Multiplies and Divides
    - 2.6. Logical Operations
        - 2.6.1. And, Or, Nor, Xor
        - 2.6.2. Sll, Sra, Srl
        - 2.6.3. Constructing Addresses and Large Constants
    - 2.7. Data Transfers
        - 2.7.1. Loads and Stores
        - 2.7.2. Alignment Requirements
        - 2.7.3. Byte Order
    - 2.8. Transfers of Control
        - 2.8.1. Jumps and Branches
        - 2.8.2. Comparisons
        - 2.8.3. Translating High-Level Control Statements
    - 2.9. Translation Process
        - 2.9.1. Memory Organization
        - 2.9.2. C/C++ Preprocessor

        2.9.3. Compiler
        2.9.4. Assembler
        2.9.5. Linker
        2.9.6. Loader
    2.10. Stored Program Concept
    2.11. Instruction Set Design Principles

3. Logic Design Slide Set
    3.1. Logic Blocks
    3.2. Expressing Logic
        3.2.1. Truth Tables
        3.2.2. Logic Equations
        3.2.3. Gates
            3.2.3.1. AND, OR, NOT, XOR, NAND, NOR
    3.3. Combinational Logic
        3.3.1. Decoders
        3.3.2. Multiplexors
        3.3.3. Array of Logic Elements
        3.3.4. Sum of Products
        3.3.5. Programmable Logic Arrays (PLAs)
        3.3.6. Read-Only Memory (ROM)
    3.4. Clocks
        3.4.1. Clock Cycle Time / Clock Period
        3.4.2. Rising and Falling Edges
        3.4.3. Edge-Triggered Clocking
        3.4.4. Synchronous System
    3.5. State Elements
        3.5.1. Latches and Flip-Flops
        3.5.2. Register Files
        3.5.3. Static Random Access Memory (SRAM)
        3.5.4. Dynamic Random Access Memory (DRAM)
    3.6. Finite State Machines

4. Single Cycle Slide Set
    4.1. Single Cycle Datapath
        4.1.1. Instruction Fetch Elements
            4.1.1.1. Instruction Memory, Program Counter (PC), Adder
        4.1.2. Data Elements
            4.1.2.1. Register File, ALU, Data Memory, Sign Extension
    4.2. Single Cycle Control
        4.2.1. ALU Control Lines
        4.2.2. Other Control Lines
        4.2.3. Control for R-format, lw, sw, beq, addiu, j, jr Instructions
    4.3. Single Cycle Overview