CDA 3101: Spring 2019
Homework 3

Total Points: 50
Due: Tuesday 04/16/2019, in class (by 4:50 PM)

Submissions are due by the beginning of class on the specified due date. Handwritten or typed solutions are acceptable. If you do write your solutions by hand, please write clearly. If the TA's cannot read your answer, they cannot give you the points.

Late submissions will be accepted with a 10% penalty by 4:50 PM on Wednesday, 04/17/2018. Late submissions should be turned in in my mailbox or under my door.

You must show how you arrived at the answer and circle your final answer where applicable!

Problem 1 - 20 points

Assume a cache with 32K blocks, a 16-word block size, and a 32-bit address. For each of the following configurations, find the total number of sets and the number of tag bits for each entry.

1. Direct-mapped
2. Four-way set associative
3. Eight-way set associative
4. Fully-associative

Problem 2 - 30 points

Assume a 4-way set-associative cache with 64 cache sets, 4 words per block, and an LRU replacement policy. For both a write-through, no write-allocate and a write-back, write-allocate cache, fill in the appropriate information for the following memory references (see slide 58-62 of Lecture 11).

R/W	**Address**	**Tag**	**Index**	**Offset**	**Result**	**Memref?**	**Update?**
W	3532						
R	3528						
W	1480						
R	1484						
R	3520						
R	13772						
W	13760						
R	448						

Table 1: Write-Through, No Write-Allocate

R/W	Address	Tag	Index	Offset	Result	Memref?	Update?
W	3532						
R	3528						
W	1480						
R	1484						
R	3520						
R	13772						
W	13760						
R	448						

Table 2: Write-Back, Write-Allocate

Problem 3 - 20 Points - Extra Credit

1. What are some advantages of the Write-Back policy over the Write-Through policy?
2. Why is it better to have associativity be a power of 2, instead of any integer value?
3. What is Paging? How is it useful?
4. How does the TLB improve memory performance?