Study Questions for Chapter 7 Part 1
Computer Organization Spring 2002

Solutions will be posted. You need not turn in any.

Problem 1
Suppose you are to implement a cache that can hold 128 KByte of data. This number is, of course, smaller than the total number of bits needed to implement the cache.

Derive the total number of bits needed to implement the cache if it:

1. is direct-mapped,

2. uses 8 word lines,

3. uses a write-back and write-allocate strategy

Problem 2
Consider the three organizations for main memory in Figure 7.13. Assume that the cache block size is 16 words.

Assume that the width of organization (b) is 4 words and that the number of banks in organization (c) is 4. Also assume that it takes 1 cycle to send the address to the memory bank(s), that the latency of each bank is 10 cycles, and the transfer time is 1 cycle.

Compute the miss penalty for each of the organizations.

Problem 3
Suppose a machine uses byte address with a k-bit address. Let the cache size (data) be $S$ bytes, the cache line size be $B = 2^b$ bytes, and suppose the cache is $A$-way associative.

Express in terms of $k, S, B, b$, and $A$ the following:

- the number of sets in the cache

- the number of index bits in the address

- and the number of bits needed to implement the cache

If you require logarithms in the expression use base 2.
Problem 4

Suppose you execute the following C code assuming no optimizations have been done.

```c
int i,j,c,stride, array[256]

*  
* other lines here of no importance
* 

for (i=0; i < 10000; i++)
{
    for (j=0; j < 256 ; j = j+stride)
    {
        c = array[j] + 5 ;
    }
}
*  
* other lines here of no importance
* 
```

Suppose integers are words and that you only consider cache activity generated by accesses to the array. Assume the cache is direct-mapped with four word blocks and holds 256 bytes of data.

What is the miss-rate as a function of stride? Consider in particular \textit{stride} = 132 and \textit{stride} = 131 then discuss what you would expect for other strides.

Would anything change if the cache were 2-way set associative?