Homework Chapter 7
Computer Organization Spring 2002

Due date: 2:30 PM, Monday, 4/15/02, TA responsible: Y. Abbas

Assumptions

- The page size in the virtual memory system is 4KB.
- The instruction TLB is direct-mapped with 2 sets and each block contains one virtual-to-physical translation.
- The virtual address has 20 bits.
- The physical address has 14 bits.

Problem 1

Justify all of your answers.

(a) How many virtual pages are in the system?
(b) How many physical pages are in the system?
(c) How many bits are in the page offset field of the virtual address?
(d) How many bits are in the page TLB index field of the virtual address?
(e) How many bits are in the page TLB tag field of the virtual address?

Problem 2

2(a)

Assume that the entries in the TLB and the page table are all initially invalid and consider the address sequence below. Assume that the replacement policy for virtual memory is LRU and that the physical pages are initially allocated in order from page 0 to page \(n - 1\) where \(n\) is the number of physical pages in the system.

For each address give the virtual page number, the page offset, the TLB tag, the TLB index, the TLB result of the access (hit or miss), the page table result (hit or miss or none, the latter being when the TLB information is enough to handle the address) and the physical page in which the address finally resides.
<table>
<thead>
<tr>
<th>Hex Virtual byte address</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x2a10</td>
</tr>
<tr>
<td>0x1004</td>
</tr>
<tr>
<td>0x20c8</td>
</tr>
<tr>
<td>0x4c04</td>
</tr>
<tr>
<td>0x3408</td>
</tr>
<tr>
<td>0x2004</td>
</tr>
<tr>
<td>0x50b4</td>
</tr>
</tbody>
</table>

2(b)

Give the final state of the TLB and the page table for the address sequence given in (a).

The TLB must contain for each entry a valid bit field, a tag field, a physical page number field. The page table must contain for each entry, a valid bit and a physical page number. You need not worry about the disk address.