Homework Chapter 4 Part 2 and 3 and Chapter 5 Part 1
Computer Organization Spring 2002
Due date: 2:30 PM, Monday, 2/18/02, TA responsible: T. Thomas

Problem 1 (20 points)
(a) (5 points) Draw a gate network that implements the switching function

\[ f(v, w, x, y, z) = (v + w)(xy + z') \]

(b) (15 points) Consider the canonical sum of products

\[ f(x, y, z) = x'y'z' + x'y'z + x'y'z + x'y'z \]

Give a simpler sum-of-products that represents the same switching function. Try and create one that has as few terms in the sum as possible and whose products involve the smallest number of switching literals. Be sure to provide a justification that the two switching expressions are the same function.

Problem 2 (25 points)
Consider the following switching expressions

\[ f(w, x, y, z) = w'y + w'xz + wy'z + x'y'z \]
\[ g(w, x, y, z) = w'y + wx'z + xy'z \]

Do the two switching expressions specify the same switching function? Justify your answer.
Problem 3 (30 points)

Recall the ALU discussed in the notes and the textbook given in Figures 4.17 and 4.18. That ALU assumes two’s complement integer encoding and implements AND, OR, ADD, SUB, and SLT. Design a modified version of the ALU that implements AND, OR, ADD, and SUB, but replaces SLT with a MIN instruction. The MIN instructions takes the two input words, A and B, and outputs the word that is smaller when interpreted as an integer. More formally,

\[
\text{if } A < B \text{ then } \\
\quad\text{Result} = A \\
\text{else} \\
\quad\text{Result} = B \\
\text{end if}
\]

Provide diagrams for the bit-slice ALU’s for your new ALU, i.e., similar to Figure 4.17, and a diagram of the overall connections for a 32-bit ALU, similar to Figure 4.18. You should also provide a table of control input settings for the 5 operations that your ALU performs: ADD, SUB, AND, OR, and MIN.

Problem 4 (25 points)

Consider the sequential machine shown in Figure 1. Suppose the combinational logic portion of the machine implements the following switching functions:

\[
\begin{align*}
z_0(b_2, b_1, b_0) &= b'_0 \\
z_1(b_2, b_1, b_0) &= b'_1 b_0 + b_1 b'_0 \\
z_2(b_2, b_1, b_0) &= b_2 b'_1 + b_2 b'_0 + b_2 b_1 b_0
\end{align*}
\]

Now suppose during clock cycle \( k \) the register contains all 0’s, i.e., \( b_2 = b_1 = b_0 = 0 \). What will the register contain during clock cycle \( k+1 \) and \( k+2 \)? Justify your answer.
Figure 1: Sequential machine for Problem 4