**Assignment #6 – Digital Logic Design II – Sequential Logic**

CDA 3100, Computer Organization I

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For this homework, you need to fill in module HW6P1 (clk, Q) and module HW6P2 (clk, X, O) in HW6.v. No other part of HW6.v needs to be changed.

**Problem 1 (50 points)** Design a circuit that has an input clk, and an output Q which has three bits. At the rising edge of the clk, the unsigned binary number represented by Q changes according to the pattern: 02371645023716450…In other words, it starts with 0 and repeats 02371645 every 8 clock cycles.

1. (10 points) Write down the next-state table.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Q2** | **Q1** | **Q0** | **D2** | **D1** | **D0** |
| 0 | 0 | 0 |  |  |  |
| 0 | 0 | 1 |  |  |  |
| 0 | 1 | 0 |  |  |  |
| 0 | 1 | 1 |  |  |  |
| 1 | 0 | 0 |  |  |  |
| 1 | 0 | 1 |  |  |  |
| 1 | 1 | 0 |  |  |  |
| 1 | 1 | 1 |  |  |  |

1. (10 points) Use Karnaugh map, derive the function for D2, D1, and D0.

D2 =

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Q2Q1  Q0 | 00 | 01 | 11 | 10 |
| 0 |  |  |  |  |
| 1 |  |  |  |  |

D1 =

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Q2Q1  Q0 | 00 | 01 | 11 | 10 |
| 0 |  |  |  |  |
| 1 |  |  |  |  |

D0 =

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Q2Q1  Q0 | 00 | 01 | 11 | 10 |
| 0 |  |  |  |  |
| 1 |  |  |  |  |

1. (10 points) Write down a Verilog module for this circuit. Use the following code as a template.

module HW6P1 (clk, Q);

input clk;

output [2:0] Q;

endmodule

1. (10 points) Run the simulation, and show the waveform here. **Please only show the signals relevant to this problem.** That is, please show only the clock and Q as an unsigned (3-bit) number. Points will be taken off if this requirement is not satisfied.
2. (10 points) Add one input “clr” to the circuit. If clr is 1, the circuit functions as previously. If “clr” is 0, Q is set to be 0 at the next rising edge. For this problem, just show the logic functions for D2, D1, and D0.

**Problem 2 (50 points)** Design a circuit that has two inputs, clk and X, and produces one output O. X may change every clock cycle, and the change happens at the falling edge. The circuit samples the input at every rising edge of the clock. If the input is 1, consider as read a 1, else read a 0. O is 1 (for one clock cycle, from positive edge to positive edge) if the last three bits read are 001, with 1 being the most recent bit.

1. (20 points) Draw the state diagram. Close to an arc, show X=1 or X=0 to indicate whether the change of state happens when X=1 or when X=0.
2. (10 points) Draw the next-state table, and derive the functions for D1 and D0. Derive the output function.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q1** | **Q0** | **X** | **D1** | **D0** |
| 0 | 0 | 0 |  |  |
| 0 | 0 | 1 |  |  |
| 0 | 1 | 0 |  |  |
| 0 | 1 | 1 |  |  |
| 1 | 0 | 0 |  |  |
| 1 | 0 | 1 |  |  |
| 1 | 1 | 0 |  |  |
| 1 | 1 | 1 |  |  |

1. (10 points) Write down a Verilog module for this circuit. Use the following code as a template.

module HW6P2 (clk, X, O);

input clk, X;

output O;

endmodule

1. (10 points) Run the simulation, and show the waveform here. **Please only show the signals relevant to this problem.** That is, please show only the clock, X and O. Points will be taken off if this requirement is not satisfied.

**Extra point problem 1** (10 points) Design a circuit that has two inputs, clk and X, and three output bits Q2Q1Q0. X may change every clock cycle where the change happens at the falling edge of the clock, and the circuit samples the input at every rising edge of the clock. Q2Q1Q0 should be the last 3 values of X, Q0 being the most recent and Q2 the least recent. Use ONLY 3 D flip-flips and wires, no any other gates or D flip-flops.

**Extra point problem 2** (10 points) Suppose we need to design a circuit that has two inputs, clk and X, and produces one output bit Y. X may change every clock cycle, where the change happens at the falling edge of the clock. The circuit samples X at every rising edge of the clock. Y should be 1 if the last 4 bits of X are “1011” from the least recent bit to the most recent bit.

Please draw the state transition diagram of this circuit. Close to an arc, show X=1 or X=0. Name the states as S0, S1,… , and so on.