

Tuning the WCET of Embedded Applications

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Why Reduce the WCET?

- more likely to meet timing constraints
- can lower clock rate to reduce power consumption

Our Approach

- interactive compilation system
- timing analyzer invoked on demand
- automatically searches for an optimization phase sequence that best reduces the WCET

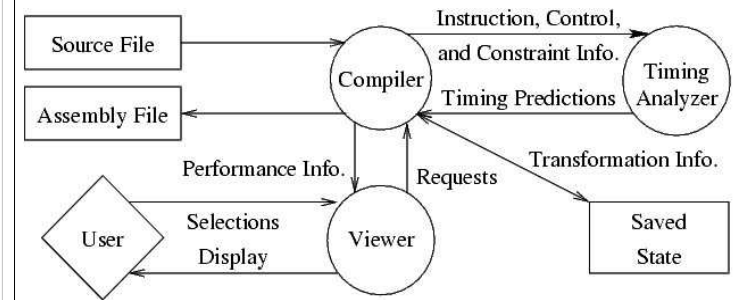
Outline of Rest of Presentation

- Related Work
- Research Framework
 - target architecture, compiler, timing analyzer
- Functionality
 - include quick demo
- Experiments
- Future Work
- Conclusions

Related Work

- methods to reduce WCET in critical sections
 - Marlowe, et al, System Integration '92
 - Hong, et al, PLDI '93
- reduce WCET on a dual instruction set processor
 - Lee, et al, WCET '03
- genetic algorithms to search for effective optimization sequences to improve speed, space, or a combination of both
 - Cooper, et al, LCTES '99
 - Kulkarni, et al, LCTES '03

Framework for This Research



Target Architecture: StarCore SC100 Processor

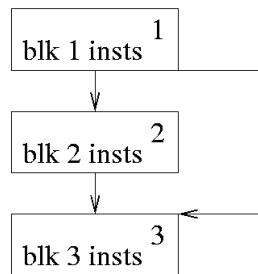
- A digital signal processor for embedded systems.
- No caches and no operating system.
- A simple five stage pipeline machine with transfer-of-control and target misalignment penalties.
- The size of instructions varies from 1 word to 5 words.

Our Timing Analyzer

- Calculates WCET for each path, loop, and function in the program.
- Features
 - WCET pipeline analysis - RTSS '95
 - WCET cache analysis - RTSS '94, RTAS '97
 - automatically calculates the number of loop iterations - RTAS '98
 - detects infeasible paths due to branch constraints - RTAS '99

Estimating WCET with Transfer of Control Penalties

- What is the WC path?



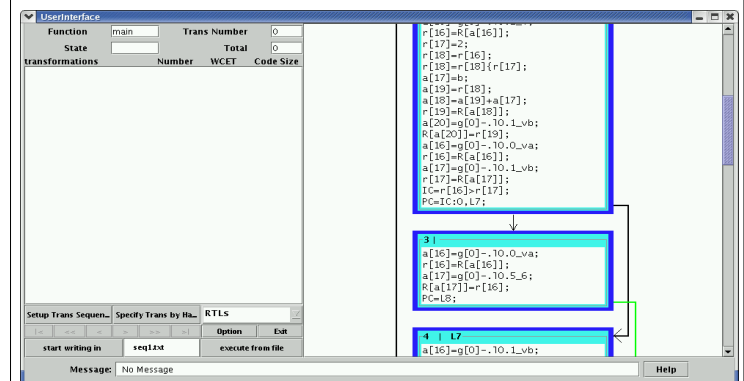
VPO Interactive System for Tuning Applications (VISTA)

- Has been previously used to tune applications for ACET and code size.
- Now interacts with our timing analyzer to determine WCET improvement.

VISTA: Functionality

- Provides a graphical display of the low-level program representation.
- Directs order and scope in which the optimization phases are applied.
- Shows feedback on the WCET and code size improvement.
- Reverses previously applied transformations.
- Uses a genetic algorithm to search for the best order of optimization phases.

Main Window of VISTA



Select Optimization Phases

Optimization Phase Selection

Branch Chaining	Dim Empty Blocks	Useless Jump Elim
Dead Code Elim	Reverse Branches	Basic Bk. Reorder
Merge Basic Blocks	Inst Selection	Fix Control Flow
Eval Order Deter	Global Inst Select	Register Assignm
Minimize Loop Jumps	Dead Variable Elim	Register Allocate
Common Subexpr Elim	Code Motion	Loop Strength Red
Recurrences	Induction Var Elim	Strength Reductio
Fix Entry Exit	Inst Scheduling	Fill Delay Slots
All Loop Transforms	Other Transform	All Loop Transform
If changes then	If changes then else	do while change
while changes do	select best from	select best combin

Optimization Phase Sequence

Inst Selection
Register Assignment
Common Subexpr Elim
Dead Variable Elim
Register Allocation
Inst Selection

3 |
r[17]=R[a[17]];
IC=r[16]>r[17];
PC=IC;O,L7;

4 | L7
a[16]=g[0]-10.0.v;a;
r[16]=R[a[16]];
a[17]=g[0]-10.5.6;
R[a[17]]=r[16];
PC=L6;

5 | L8
a[16]=g[0]-10.1.v;b;
r[16]=R[a[16]];
a[17]=g[0]-10.5.6;
R[a[17]]=r[16];

Main Window of VISTA (again)

Function

Function	State	Trans Number	Total	WCT	Code Size
main		113	113		
Transformations		Number	WCT	Code Size	
Inst Selection		24	76.23	62.92	
Register Assignment		9	76.23	62.92	
Common Subexpr Elim		12	63.36	50.56	
Dead Variable Elim		6	62.37	49.43	
Register Allocation		7	44.55	49.43	
Inst Selection		(45)	45	36.63	41.57

3 |
r[1]=r[0];
PC=L8;

4 | L7
r[1]=r[1];

5 | L8
r[1]=r[1];
r[8]=r[8]+r[1];
r[0]=r[8];
r[1]=r[3];
PC=IC;O,L10;

6 |
r[1]=r[0];
PC=L11;

7 | L10
r[1]=r[1];

8 | L11

Select the Candidate Phases

Optimization Phase Selection

Branch Chaining	Dim Empty Blocks	Useless Jump Elim
Dead Code Elim	Reverse Branches	Basic Bk. Reorder
Merge Basic Blocks	Inst Selection	Fix Control Flow
Eval Order Deter	Global Inst Select	Register Assignm
Minimize Loop Jumps	Dead Variable Elim	Register Allocate
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Recurrences	Induction Var Elim	Strength Reductio
Fix Entry Exit	Inst Scheduling	Fill Delay Slots
All Loop Transforms	Other Transform	All Loop Transform
If changes then	If changes then else	do while change
while changes do	select best from	select best combin

Optimization Phase Sequence

select best combination
(s) - Inst Selection
(c) - Common Subexpr Elim
(b) - Dead Variable Elim
(k) - Register Allocation
end select@00

3 |
r[8]=r[8]+a[17];
r[19]=R[a[18]];
a[20]=g[0]-10.1.v;b;
R[a[20]]=r[19];
a[16]=g[0]-10.0.v;a;
r[16]=R[a[16]];
a[17]=g[0]-10.1.v;b;
r[17]=R[a[17]];
IC=r[16]>r[17];
PC=IC;O,L7;

4 | L7
a[16]=g[0]-10.0.v;a;
r[16]=R[a[16]];
a[17]=g[0]-10.5.6;
R[a[17]]=r[16];
PC=L6;

5 | L8
a[16]=g[0]-10.1.v;b;
r[16]=R[a[16]];
a[17]=g[0]-10.5.6;
R[a[17]]=r[16];

Selecting Search Options

Sel... Comb Query

No. of Phases: 4

Sequence Length: 5

Weight Factors:
WCT: 50
Code Size: 50

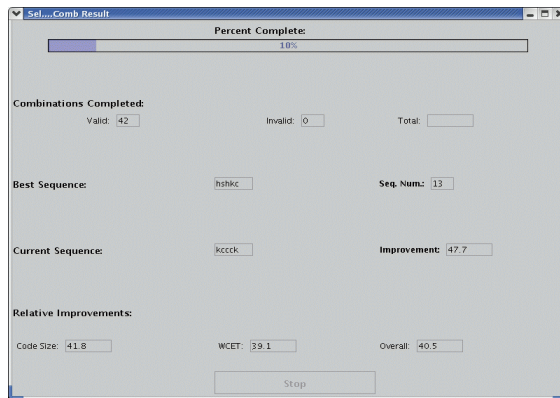
Search Option:
 Exhaustive Search
 Biased Sampling Search
 Permutation Search

Population Size: 20

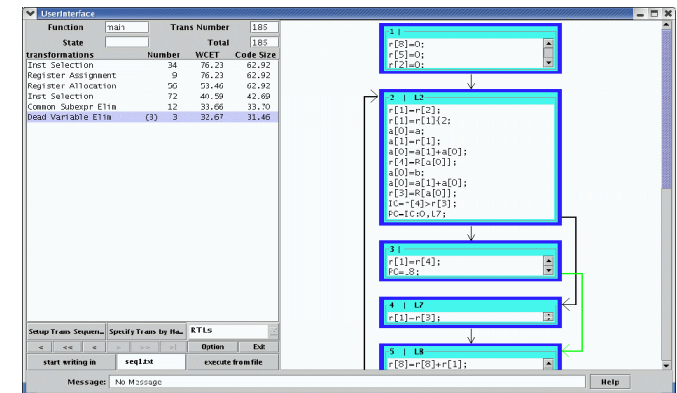
Number of Generations: 20

ok cancel help

Window Showing the Search Status



GA Results



Experiments

- Evaluated effectiveness of VISTA's GA search for improving WCET.
 - Each phase is considered a gene.
 - Each sequence of phases is considered a chromosome.
- Much faster to interact with a timing analyzer to obtain WCET than a simulator to obtain ACET.

Candidate Optimization Phases

- | | |
|----------------------------------|-----------------------------|
| branch chaining | loop transformations |
| remove useless blocks | merge basic blocks |
| remove unreachable code | evaluation order |
| code | determination |
| common subexpression elimination | dead assignment elimination |
| register allocation | strength reduction |
| block reordering | reverse jumps |
| minimize loop jumps | instruction selection |
| remove useless jumps | |

Genetic Algorithm (GA) Parameters

- Sequence length (chromosome) is 1.25 times the number of phases that were successfully applied by the batch compiler.
- Population size: 20 sequences
- Generations: 200
- 4 sequences are replaced by crossover operations.
- Mutation rate: 10% lower half, 5% upper half
- 3 different fitness criteria:
 - 100% WCET, 100% code size, 50% WCET and 50% code size

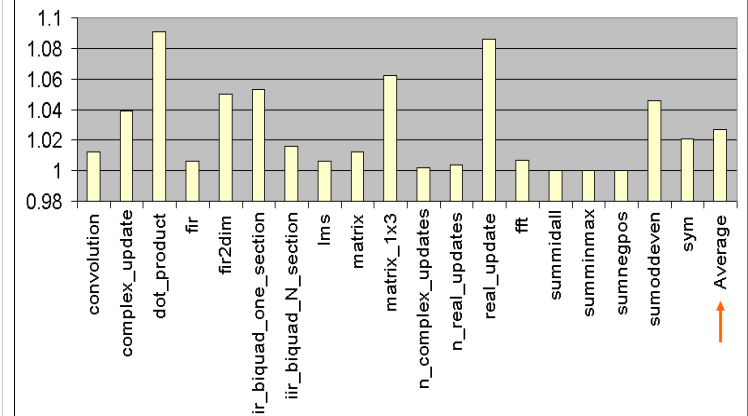
DSPstone Benchmarks

Program	Description
convolution	perform a convolution filter
complex_update	performs a single mac operation on complex values
dot_product	computes the product of two vectors
fir	perform a FIR filter
fir2dim	perform a FIR filter on a 2D image
iir_biquad_one_section	perform a IIR filter on one section
iir_biquad_N_sections	perform a IIR filter on multiple sections
lms	least mean square adaptive filter
matrix	computes matrix product of two 10x10 matrices
matrix_1x3	computes matrix product of 3x3 and 3x1 matrices
n_complex_updates	performs a mac operation on an array of complex values
n_real_updates	performs a mac operation on an array of data
real_update	performs a single mac operation

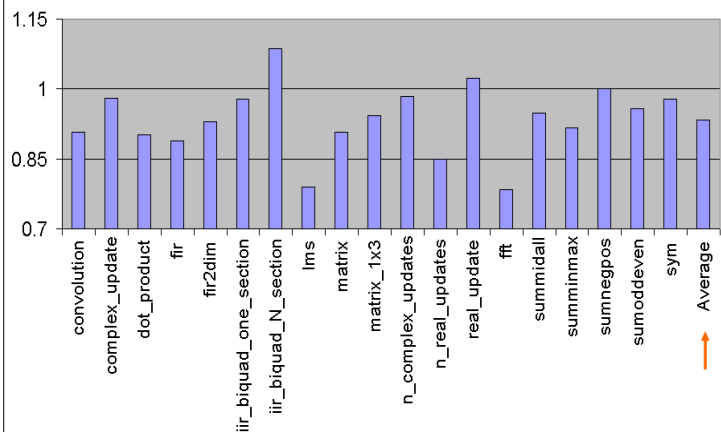
Other Benchmarks

Program	Description
fft	128 point complex FFT
summidall	sums the middle half and all elements of a 1000 integer vector
summinmax	sums the minimum and maximum of the corresponding elements of two 1000 integer vectors
sumnegpos	sums the negative, positive, and all elements of a 1000 integer vector
sumoddeven	sums the odd and even elements of a 1000 integer vector
sym	test if a 100x100 matrix is symmetric

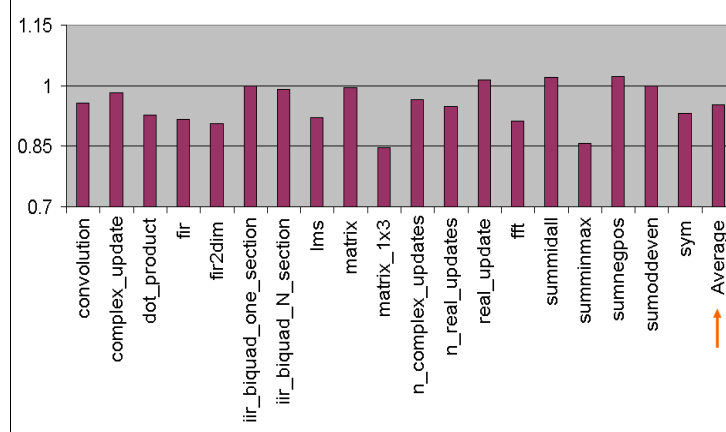
WCET vs. Observed Cycles



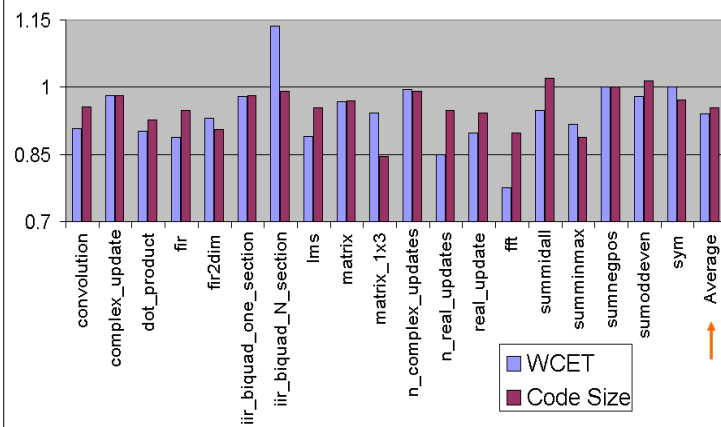
Tuning for WCET



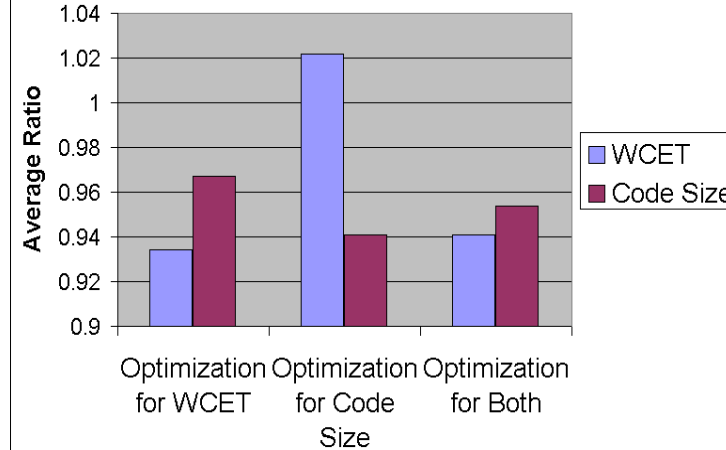
Tuning for Code Size



50% WCET and 50% Code Size



Result of the Three Fitness Criteria



Future Work

- Develop compiler optimizations that use worst-case path information to improve WCET.
- Example:
 - change order of basic blocks to reduce transfer of control penalties for worst-case paths

Conclusions

- Developed the first system where a compiler can invoke a timing analyzer on demand.
- Showed that WCET can be used as a fitness value to a genetic algorithm to find an effective optimization sequence.
- WCET and code size were simultaneously improved by 6% and 5%, respectively.