**Curriculum Vitae**

***Gary Scott Tyson***

*Jan 1, 2009*

## GENERAL INFORMATION


University Address: Computer Science Department
College of Arts and Science
163 Love Building
Florida State University
Tallahassee, Florida 32306-4530
Phone: (850) *644-3088* - FAX: (850) *644-0058*

E-Mail Address: *tyson@cs.fsu.edu*

Web Site: *http://www.cs.fsu.edu/~tyson*


## Professional Preparation

*February 1997* *Doctor of Philosophy*, *University of California*, *Davis*. *Major: Computer Science*, *Minor: Robotics.* Dissertation: "Evaluation of a Scalable Decoupled Microprocessor Design"

*January 1988* *Master's in Science, California State University, Sacramento. Major: Computer Science.* Thesis: "A Distributed Robot Control Environment"

*June 1986* *Bachelor's in Science*, *California State University, Sacramento. Major: Computer Science, Minor: Mathematics.*

## Professional Experience

*8/2003 – 8/2009*[1] *Associate Professor – Computer Science Department*, *College of Arts and Science*, *Florida State University.* Taught graduate and undergraduate courses in Computer Science. Advised graduate students. Performed departmental, university, national and international service. Served as interim associate chairman for Computer Science department from 9/2006 – 8/2007.

[1]Promotion to Professor (Computer Science Department / FSU) Effective 8/2009

*1/1997 – 8/2003* <u>*Assistant Professor*</u> *– Department of Electrical Engineering and Computer Science*, *College of Engineering*, *University of Michigan.* Taught graduate and undergraduate courses in Computer Science. Advised graduate students. Performed departmental, university, national and international service.

*8/1995 – 12/1996* <u>*Acting Assistant Professor*</u> *– Computer Science Department*, *College of Engineering*, *University of California – Riverside.* Taught graduate and undergraduate courses in Computer Science. Advised graduate students. Performed departmental, national and international service.

*8/1993 – 6/1994* <u>*Associate In Computer Science*</u> *– Computer Science Department*, *College of Engineering*, *University of California – Davis.* Taught undergraduate courses in Computer Science.

*8/1988 – 06/90* <u>*Lecturer*</u> *– Computer Science Department*, *College of Engineering*, *California State University – Sacramento.* Taught graduate and undergraduate courses in Computer Science.

## Honors and Awards

FSU Graduate Student Research and Creativity Award, for Steve Hines, Florida State University, 2008.

Developing Scholar Award, Florida State University, 2007.

Horace H. Rackham Distinguished Dissertation Award, for Hsien-Hsin Lee, University of Michigan, 2001.

Best Paper Award. The 33rd ACM/IEEE International Symposium on Microarchitecture (MICRO-33), 2000.

National Science Foundation CAREER award, 1997.

## Membership in Professional Organizations

Association of Computing Machinery
IEEE
Tau Beta Pi
Upsilon Pi Epsilon

## TEACHING

### Courses Taught

*Courses taught at Florida State University: (ID: Title (semesters taught))*

CDA 3101: Computer Organization (S04, S06, S07, S08)
CDA 4150: Computer Architecture (F05, F07, F08)
CDA 5155: Computer Architecture (F03, F05, F07, F08)
CGS 5267: Computer Organization(S04, S06, S07, S08)
CIS 4900: Honors Work (S07)
CIS 4933: Honors Work (S07, F07, S08, F08)
CIS 5900: Advanced Computer Architecture (S05)
CIS 5900: Embedded Systems (S06)
CIS 5935: Introduction to Research (F06)
CIS 5970: Thesis (S06, F06, S07, F07, S08, F08)
CIS 6900: Architecture Research (S04, F04, S05, F05, S06, F06, S07, F07, S08, F08)
CIS 6935: Topics in Architecture (F04)
CIS 6980: Dissertation (S07, F07)
CIS 8962: PhD Qualifying Exam (S07)
CIS 8976: Master's Thesis Defense (S07, F07)
CIS 8985: Dissertation Defense (S08)
CEN 4012: Software Engineering Project (S05)
COP 3330: Object Oriented Programming (S05)

*Courses taught prior to joining Florida State University:*

1997-2003: University of Michigan
- EECS 280: Data Structures (multiple times)
- EECS 370: Computer Organization (multiple times)
- EECS 470: Computer Architecture
- EECS 570: Advanced Computer Architecture (multiple times)
- EECS 573: Advanced Compilers (multiple times)

1995-1996: University of California – Riverside
- CS 161: Design and Architecture of Computer Systems (multiple times)
- CS 203: Advanced Computer Architectures
- CS 230: Computer Graphics

1993-1994: University of California – Davis
- ECS 30: Introduction to Programming (multiple times)

1988-1990: California State University, Sacramento
- CSC 15: Programming Concepts (in C)
- CSC 60: Introduction to Unix Programming (multiple times)

CSC 68: Fortran
CSC 130: Systems Programming (multiple times)
CSC 239: Advanced Unix Programming
CSC 258: Robotics Laboratory

**New Course Development**

CIS 5900: Advanced Computer Architecture (S05)
CIS 5900: Embedded Systems (S06)

**Chair of Doctoral Dissertation Supervisory Committees**

Stephen Hines, 2008, "Improving Processor Efficiency through Enhanced Instruction Fetch" Co-advised with Professor David Whalley

Allen Cheng, 2006, "Application Specific Architecture Framework for High-Performance Low-Power Embedded Computing"

Mike Geiger, 2006, "Improving Performance and Energy Consumption in Region-Based Caching Architectures"

Viji Srinivasan, 2001, "Hardware Solutions to Reduce Effective Memory Access Time"

Hsien-Hsin Lee, 2001, "Improving Energy and Performance of Data Cache Architectures by Exploiting Memory Reference Characteristics"

Edward Tam, 1999, "Improving Cache Performance Via Active Management" Co-advised with Professor Edward Davidson

Jude Rivers, 1998, "Performance Aspects of High-Bandwidth Multi-Lateral Cache Organizations" Co-advised with Professor Edward Davidson

*In progress:*

Yuval Peress, est 2009, working title: "Clustering Computational Resource in Heterogeneous Processor Architectures"

Paul West, est 2009, working title: "Next Generation Performance Counters for Multi-core Processors"

Justin Fincher, est 2011, working title: "Categorizing Epigenetic Markers in Cell Differentiation"

Ian Finlayson, est 2011, working title: "Static Pipelined Architectures for Low Power Embedded Systems" Co-advised with Professor David Whalley

Daniel Chang, est 2012, working title: "Security Enhancement using Program Differentiation"

Peter Gavins, est 2012, working title: "Instruction Fetch Optimization for Multiple Processor Core Systems"

Alexandro Cabrera, est 2012, working title: "Mobile Software Systems"

Justin Marshall, est 2012, working title: "Utilizing Mobile Systems in Medicine"

**Member of Doctoral Dissertation Supervisory Committees**

Todd Angel, 2007
Prasad Kulkarni, 2007
Keith Haynes, 2006
R. Whaley, 2004
William Kreahling, 2004
David Greene, 2003
Mathew Postiff, 2001
Krisztian Flautner, 2001
Charles Lefurgy, 2000
James Dundas, 1998
Bruce Jacob, 1997

**Chair of Master's Thesis Supervisory Committees**

Yuval Peress, 2008
Paul West, 2008
Kelley Jones, 2007 co-advised with David Whalley
Mark Searles, 2006 co-advised with David Whalley
Chris Zimmer, 2006 co-advised with David Whalley
Brian Harvey, 1996
Kelsey Lick, 1996

**Chair of Honors Thesis Supervisory Committees**

Michael Serritella, 2008
Yugala Priti Meier, 2007

## SCHOLARLY OR CREATIVE ACTIVITIES

**Publications** (my students names are in **bold**)

### Journal Articles Published

1. Prasad Kulkarni. David Whalley, Gary Tyson and Jack Davidson, "Practical Exhaustive Optimization Phase Order Exploration and Evaluation," accepted in ACM Transactions on Architecture and Code Optimization. *In press*. Acceptance August 2008.

2. **M.J. Geiger**, S.A. McKee, G.S. Tyson, "Specializing Cache Structures for High Performance and Energy Conservation in Embedded Systems," Transactions on High Performance Embedded Architectures and Compilers (HiPEAC), vol. 1, no. 1, 2007, pages 50-90.

3.M. Bhadauria, S.A. McKee, K. Singh, G.S. Tyson, "Data Cache Techniques to Save Power and Deliver High Performance in Embedded Systems," Transactions on High Performance Embedded Architectures and Compilers (HiPEAC), vol 2. no. 1, 2007, pages 62-81.

4. **Allen Cheng** and Gary Tyson, "High Quality ISA Synthesis for Low-Power Cache Designs in Embedded Processors," IBM Journal of Research and Development (JRD), Vol 50, No 1, April 2006.

5. **Allen Cheng** and Gary Tyson, "An Energy Efficient Instruction Set Synthesis Framework for Low Power Embedded Systems Designs," IEEE Transactions on Computers, Vol 54, No. 6, pp. 698-713, June 2005.

6. **Viji Srivivasan**, Edward Davidson and Gary Tyson, "A Prefetch Taxonomy," IEEE Transactions on Computers, 53(2), pp. 126-140, February 2004.

7. **Hsien-Hsin Lee**, Gary Tyson and Matthew Farrens, "Improving Bandwidth Utilization Using Eager Writeback," Journal of Instruction Level Parallelism, 3(1), pp. 1-22, October 2001.

8. Gary Tyson, **Mikhail Smelyanskiy** and Edward Davidson, "Evaluating the Use of Register Queues in Software Pipelined Loops," IEEE Transactions on Computers, 50(8), pp. 769-783, August 2001.

9. **Edward Tam, Jude Rivers, Viji Srivivasan**, Gary Tyson and Edward Davidson, "Active Management of Data Caches by Exploiting Reuse Information," IEEE Transactions on Computers, 48(11), pp. 1244-1259, 1999.

10.Gary Tyson and Todd Austin, "Memory Renaming: Fast, Early and Accurate Processing of Memory Communication," International Journal of Parallel Programming 27(5), pp. 357-380, October 1999.

11.Matt Postiff, Gary Tyson and Trevor Mudge, "Performance Limits of Trace Caches," Journal of Instruction Level Parallelism, 1(1), pp. 1-17, October 1999.

12.Gary Tyson, Matthew Farrens, John Matthews, Andrew Pleszkun, "Managing Data Caches using Selective Cache Line Replacement," International Journal of Parallel Programming, 25(3), pp. 213-242, 1997.

13.Gary Tyson and Matthew Farrens, "Evaluating the Effects of Predicated Execution on Branch Prediction," International Journal of Parallel Programming, 24(2), pp. 159-186, 1996.

14. Gary Tyson and Matthew Farrens, "Code Scheduling for Multiple Instruction Stream Architectures," International Journal of Parallel Programming, 22(3), pp. 243-272, 1994.

## Books Published

15. Ann Ford, Toby Teorey, and Gary Tyson, "C++ Debugging Guide", ISBN: 0536987653; Published: August 2005, Prentice Hall.

16. Sandy Bartlett, Ann Ford, Toby Teorey, and Gary Tyson, "Java Debugging Guide", ISBN: 0536987041; Published: August 2005, Pearson Publishing.

17. Ann Ford, Toby Teorey, Sandy Bartlett, Gary Tyson, "Practical Debugging in Java", ISBN: 0131427814; Published: July 30, 2003, Prentice Hall.

## Proceedings Published

18. **Paul West**, Gary Tyson, and Sally McKee, "Core Monitors: Monitoring Performance in Multicore Processors," *Accepted for publication* ACM International Conference on Computing Frontiers", Ischia, Italy.

19. Renato J. O. Figueiredo, P. Oscar Boykin, José A. B. Fortes, Tao Li, Jie-Kwon Peir, David Wolinsky, Lizy Kurian John, David R. Kaeli, David J. Lilja, Sally A. McKee, Gokhan Memik, Alain Roy, and Gary S. Tyson," Archer: A Community Distributed Computing Infrastructure for Computer Architecture Research and Education," CoRR 0807.1765: (2008)

20.David Whalley and Gary Tyson, "Enhancing the Effectiveness of Utilizing and Instruction Register File," Proceedings of the National Science Foundation Principal Investigators workshop, April 2008.

21.M. Bhadauria, S.A. McKee, K. Singh, G. Tyson, "Leveraging High Performance Cache Techniques in Mobile Embedded Systems," Proc. International Conference on High Performance Embedded Architectures and Compilers, Ghent, BE, February 2007.

22. **S. Hines**, D. Whalley, G. Tyson, "Guaranteeing Hits to Improve the Efficiency of a Small Instruction Cache" in the Proceedings of the International Symposium on Microarchitecture December 2007, pages 433-444.

23. **C. Zimmer, S. Hines**, P. Kulkarni, G. Tyson, D. Whalley, "Facilitating Compiler Optimizations through the Dynamic Mapping of Alternate Register Structures" in the Proceedings of the International

IEEE/ACM Conference on Compilers, Architecture, and Synthesis for Embedded Systems, October 2007.

24. **S. Hines**, G. Tyson, D. Whalley, "Addressing Instruction Fetch Bottlenecks by Using an Instruction Register File" in the Proceedings of the ACM Conference on Languages, Compilers, and Tools for Embedded Systems, June 2007, pages 165-174.

25.P. Kulkarni, D. Whalley and G. Tyson, “Evaluating Heuristic Optimization Phase Order Search Algorithms,” the Proceedings of the 2007 International Symposium on Code Generation and Optimization, March 2007.

26. M. Bhadauria, S.A. McKee, K. Singh and G. Tyson, “A Precisely Tunable Drowsy Cache Management Mechanism” the proceedings of the third Watson conference on Interactions between Architecture, Circuits and Compilers ($PAC^2$), October 2006.

27. **S. Hines**, D. Whalley and, G. Tyson, "Adapting Compilation Techniques to Enhance the Packing of Instructions into Registers," Proceedings of the International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, October 2006.

28. **C. Zimmer**, G. Tyson, and D. Whalley, "Application Configurable Processors" Proceedings of the ACM SIGPLAN/SIGBED Conference on Language, Compilers, and Tools for Embedded Systems, June 2006, pages 49-52.

29. **M. Searles**, D. Whalley, and G. Tyson, "Exploitation of a Large Data Register File," Proceedings of the ACM SIGPLAN/SIGBED Conference on Language, Compilers, and Tools for Embedded Systems, June 2006, pages 37-40.

30.P. Kulkarni, D. Whalley, G. Tyson and J. Davidson, "In Search of Near-Optimal Optimization Phase Orderings," Proceedings of the ACM Conference on Languages, Compilers, and Tools for Embedded Systems, June 2006, pages 83-92.

31. W. Kreahling, **S. Hines**, D. Whalley and G. Tyson, "Reducing the Cost of Conditional Transfers of Control by Using Comparison Specifications," Proceedings of the ACM Conference on Languages, Compilers, and Tools for Embedded Systems, June 2006, pages 64-71.

32.Prasad Kulkarni, David Whalley, Gary Tyson and Jack Davidson, “Exhaustive Optimization Phase Order Space Exploration,” proceedings of the IEEE/ACM International Symposium on Code Generation and Optimization, March 2006, pages 306-318.

33. **Mike Geiger**, Gary Tyson and Sally McKee, “Beyond Basic Region Caching: Specializing Cache Structures for High Performance and Energy Conservation”, proceedings of the International Conference on High Performance Embedded Architectures and Compilers, November 2005.

34. **Steve Hines**, Gary Tyson and David Whalley, “Reducing Instruction Fetch Cost by Packing Instructions into Register Windows,” proceedings of the 38th Annual International Symposium on Microarchitecture (MICRO38), November 2005. [Acceptance rate: 19% (29/147)]

35. **Steve Hines**. Gary Tyson and David Whalley, "Improving the Energy and Execution Efficiency of a Small Instruction Cache by Using an Instruction Register File," proceedings of the second Watson conference on Interactions between Architecture, Circuits and Compilers (PAC$^2$), pp. 160-169, September 2005. [Acceptance rate: 44% (21/47)]

36. **Steve Hines, Joshua Green**, Gary Tyson and David Whalley "Improving Program Efficiency by Packing Instructions into Registers", proceedings of the 2005 IEEE International Symposium on Computer Architecture (ISCA), June 2005. [Acceptance rate: 23% (45/194)]

37. **Mike Geiger**, Gary Tyson and Sally McKee, "Drowsy Region Based Caches: Minimizing both Dynamic and Static Power Dissipation", proceedings of the 2005 ACM International Conference on Computing Frontiers, May 2005.

38. **Allen Cheng** and Gary Tyson, "PowerFITS: Reduce Dynamic and Static I-Cache Power Using Application Specific Instruction Set Synthesis", proceedings of the 2005 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), March 2005.

39. **Allen Cheng**, Gary Tyson and Trevor Mudge, "Application Specific Instruction Set Synthesis to Reduce Instruction Cache Power in Embedded Processors," proceedings of the first Watson conference on Interactions between Architecture, Circuits and Compilers (PAC$^2$), October 2004. [Acceptance rate: 38%]

40. **Mike Geiger** and Gary Tyson, "Reducing Static Power Dissipation on Region Based Caches," proceedings of the first Watson conference on Interactions between Architecture, Circuits and Compilers (PAC$^2$), October 2004. [Acceptance rate: 38%]

41. **Allen Cheng**, Gary Tyson and Trevor Mudge, "FITS: Framework Based Instruction Set Tuning Synthesis for Embedded Application Specific Processors", proceedings of the 41$^{st}$ Design Automation Conference, pp. 940- 943, June 2004. [Acceptance rate: 30%]

42. **Allen Cheng**, Gary Tyson and Trevor Mudge, "FITS: Increasing Code Density for Embedded Systems with a Cost-Effective 16-bit Synthesis Technique", Digest of the 2$^{nd}$ workshop on Optimization for DSP and Embedded Systems (ODES-2), March 2004.

43. **Ramu Pyreddy** and Gary Tyson, "Exploiting Load Latency Tolerance for Relaxing Cache Design Constraints," Proceedings of the Workshop on Complexity-Effective Design, in conjunction with the 29th International Symposium on Computer Architecture, pp. 1-15, June 2002.

44. **Edward S. Tam**, Stevan A. Vlaovic, Gary S. Tyson and Edward Davidson, "Allocation by Conflict: A Simple, Effective Cache Management Scheme," IEEE International Conference of Computer Design, pp. 133-140, Sept 2001. [Acceptance rate: 24%]

45. **Ramu Pyreddy** and Gary Tyson, "Evaluating Design Tradeoffs in Dual Speed Pipelines," Proceedings of the Workshop on Complexity-Effective Design, in conjunction with the 28th International Symposium on Computer Architecture, pp. 1-8, June 2001. [Acceptance Rate: unknown]

46. **Viji Srivivasan**, Edward Davidson, Gary Tyson, Mark Charney and Thomas Puzak, "Branch History Guided Instruction Prefetching," Seventh International Symposium on High Performance Computer Architecture, pp. 291-300, January 2001. [Acceptance rate: 24% (26/108)]

47. **Hsien-Hsin Lee, Mikhail Smelyanski**, Chris Newburn and Gary Tyson, "Stack Value File: Custom Microarchitecture for the Stack," Seventh International Symposium on High Performance Computer Architecture, pp. 5-14, January 2001. [Acceptance rate: 24% (26/108)]

48. Steve Vlaovic, Edward Davidson and Gary Tyson, "Improving BTB performance in the presence of DLLs," 33rd Annual International Symposium on Microarchitecture, pp. 77-86, December 2000. [Acceptance rate: 28% (31/110)]

49. **Hsien-Hsin Lee**, Gary Tyson and Matthew Farrens, "Eager Writeback - a Technique for Improving Bandwidth Utilization," 33rd Annual International Symposium on Microarchitecture, pp. 11-20, December 2000. [Acceptance rate: 28% (31/110)] **[BEST PAPER AWARD]**

50. **Hsien-Hsin Lee** and Gary Tyson, "Region-based caching: An energy-delay efficient memory architecture for embedded processors," International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES 2000), pp. 120-127, November 2000. [Acceptance rate: 30%]

51. **Mikhail Smelyanskiy**, Gary Tyson and Edward Davidson, "Register Queues: A New Hardware/Software Approach to Efficient Software Pipelining," International Conference on Parallel Architectures and Compilation Techniques (PACT 2000), pp. 3-12, October 2000. [Acceptance rate: 21% (22/107)]

52. **Murali Annavaram**, Gary S. Tyson and Edward S. Davidson, "Instruction Overhead and Data Locality Effects in Superscalar Processors," IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), pp. 95-100, April 2000. [Acceptance rate: 29% (21/72)]

53. **Hsien-Hsin Lee**, Youfeng Wu, and Gary Tyson, "Quantifying Instruction-Level Parallelism Limits on an EPIC Architecture," IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), pp. 21-27, April 2000.

54. Matthew A. Postiff, David A. Green, Gary S. Tyson and Trevor N. Mudge, "Limits of Instruction Level Parallelism in SPEC95 Applications," Computer Architecture News, 27(1), March 1999.

55. Krisztian Flautner, Gary S. Tyson and Trevor Mudge, "MirvSim: A high level simulator integrated with the Mirv compiler," Computer Architecture News, 27(1), March 1999.

56.Glenn Reinman, Brad Calder, Dean Tullsen, Gary Tyson and Todd Austin, "Classifying Load and Store Instructions for Memory Renaming," ACM International Conference on Supercomputing, pp. 399-407, June 1999. [Acceptance rate: 32% (57/180)]

57. Sangwook P. Kim and Gary S. Tyson, "Analyzing the Working Set Characteristics of Branch Execution," Proceeding of the 31th Annual Symposium on Microarchitecture, pp. 49-58, December 1998. [Acceptance rate: 26% (28/108)]

58. Matthew A. Postiff, David A. Green, Gary S. Tyson and Trevor N. Mudge, "Limits of Instruction Level Parallelism in SPEC95 Applications," Proceedings of the 3rd Workshop on Interaction between Compilers and Computer Architectures, October 1998. [Acceptance Rate: unknown]

59. Krisztian Flautner, Gary S. Tyson and Trevor Mudge, "MirvSim: A high level simulator integrated with the Mirv compiler," Proceedings of the 3rd Workshop on Interaction between Compilers and Computer Architectures, October 1998. [Acceptance Rate: unknown]

60. **Edward S. Tam, Jude A. Rivers, Vijayalakshmi Srivivasan**, Gary S. Tyson and Edward S. Davidson, "Evaluating the Performance of Active Cache Management Schemes," Proceedings of the 1998 IEEE International Conference on Computer Design, pp. 368-375, October 1998. [Acceptance rate: 63% (83/126)]

61. **Edward S. Tam, Jude A. Rivers**, Gary S. Tyson and Edward S. Davidson, "mlcache: A Flexible Multi-Lateral Cache Simulator," Proceedings of the 6th International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS '98), pp. 19-26, July 1998.

62. **Jude A. Rivers, Edward S. Tam**, Gary S. Tyson, Edward S. Davidson and Matthew Farrens, "Utilizing Reuse Information in Data Cache Management," Proceedings of the 12th ACM International Conference on Supercomputing, pp. 449-456, July 1998.

63. **Jude A. Rivers**, Gary S. Tyson, Edward S. Davidson and Todd M. Austin, "On High-Bandwidth Data Cache Design for Multi-Issue Processors," Proceeding of the 30th Annual Symposium on Microarchitecture, pp. 46-56, December 1997. [Acceptance rate: 34% (35/103)]

64. Gary Tyson, Matthew Farrens, John Matthews and Andrew R. Pleszkun, "A Modified Approach to Cache Management," Proceeding of the 28th Annual Symposium on Microarchitecture, pp. 93-103, November 1995. [Acceptance rate: 24% (22/90)]

65. Gary Scott Tyson, "The Effects of Predicated Execution on Branch Prediction," Proceeding of the 27th Annual Symposium on Microarchitecure, pp. 196-206, November 1994. [Acceptance rate: 29% (18/63)]

66. Matthew Farrens, Gary Tyson and Andrew R. Pleszkun, "A Study of Single-Chip Processor/Cache Organizations," Proceeding of the 21st Annual Symposium on Computer Architecture, pp. 338-347, April 1994. [Acceptance rate: 24% (34/143)]

67. Gary Tyson and Matthew Farrens , "Techniques for Extracting Instruction Level Parallelism on MIMD Machines," Proceeding of the 26th Annual Symposium on Microarchitecture, pp. 128-137, December 1993. [Acceptance rate: 33% (21/63)]

68. Gary S. Tyson, Robert J. Shaw and Matthew K. Farrens, "An Interactive Compiler Development System," Proceedings of the first TCL/TK workshop, pp. 136-138, June 11, 1993.

69. Gary Tyson, Matthew Farrens and Andrew R. Pleszkun , "MISC: A Multiple Instruction Stream Computer," Proceeding of the 25th Annual Symposium on Microarchitecture, pp. 193-199, December 1992. [Acceptance rate: 29% (21/72)]

70. Matthew Farrens, Arvin Park and Gary Tyson , "Modifying VM Hardware to Reduce Address Pin Requirements," Proceeding of the 25th Annual Symposium on Microarchitecture, pp. 210-215 December 1992. [Acceptance rate: 29% (21/72)]

71. Matthew Farrens, Arvin Park, Rob Fanfelle, Pius Ng and Gary Tyson , "A Partitioned TLB Approach to Reduced Address Bandwidth," Proceeding of the 19th Annual Symposium on Computer Architecture, pp. 435, May 1992. [Acceptance rate: 43% (75/173) abstract]

## Invited Keynote and Plenary Presentations

Gary Tyson, Keynote Address: Interaction Between Compiler And Architecture in General Purpose Processor Design", Internation Symposium on System Synthesis, 1996. Scope of Conference: International.

## Inventions

## Patented Inventions

David Whalley and Gary Tyson, US Patent Application No. 11/240,881 "Packing Instructions into an Instruction Register File"

Gary Tyson, Steve Hines, David Whalley, US Patent Application No. 60989352, "Lookahead Instruction Fetch"

## Contracts and Grants

## Contracts and Grants Funded

Sun: Low Power Instruction Fetch on Sun Niagara T2 Processors
4/2008: $54,000 equipment

FSU: GAP: Tagless Hit Instruction Cache
5/2007 to 5/2008 $44,000
PI: David Whalley

NSF: CRI:CRD: Collaborative Research: Archer – Seeding a Community-based Computing Infrastructure for Computer Architecture Research and Education
5/2008 to 8/2008 $995,787 (FSU portion $67,995)
7 Co-PIs at other institutions

FSU: GAP: Instruction Register File
5/2007 to 5/2008 $30,000

Co-PI: David Whalley

NSF: CSR-EHS: Enhancing the Effectiveness of Utilizing an IRF
9/2006 to 8/2008 $290,000 +$12,000 REU
PI: David Whalley

FSU: PEG: Expanding the Use of Registers in Embedded Systems
6/2005 to 5/2007 $100,000
Co-PI: David Whalley

NSF: Collaborative Research: ST-HEC: Scalable, Interoperable Tools to Support Autonomic Optimization of High-end Applications 1/2005 to 11/2008
$750,000 ($190,000 to FSU) Cornell PI: Sally McKee @ ECE Department, Cornell University and Oregon PI: Allen Malony @ CS Department, University of Oregon

IBM UPP: Novel Memory-System Architectures Including High Bandwidth Multi-Lateral Caches on Very Large Secondary and Tertiary Cache Structures 12/1998 to 8/2003 $70,000

IBM UPP: Binary Recompilation and Combined Compiler Architecture Enhancements to Improve the Performance of Legacy Binaries, 12/1998 to 8/2004, $70,000NSF: Multi-level Parallel Execution on Decoupled Systems 8/1998 to 7/2002 $185,936

NSF: CAREER: Improving Compiler/Architecture Synergy 5/1998 to 5/2003 $200,000

Intel: Utilization of Advanced Intel Based Platforms in Computationally Demanding Tasks (numerous coPIs) 8/1997 to 6/2000 $5,994,081 equipment

**Contracts and Grants Submitted**

NSF: Increasing Participation in Computer Science 3/2008 to 6/2012 $600,000
Co-PIs: Davis Whalley, Ted Baker, Robert van Engelen, Piyush Kumar

## SERVICE

### Florida State University

**University**

FSU Faculty Senator, 2008

FSU Faculty Senator, 2007

FSU University Council on Research and Creativity, 2007

Chair, CRC Planning Grant (Science area) Sub-committee, 2007
FSU Faculty Senator, 2006
FSU University Council on Research and Creativity, 2006
Chair, CRC Planning Grant (Science area) Sub-committee, 2006
Member, Computer and Information Resources Committee, 2006
FSU Faculty Senator, 2005
Member, FSU University Council on Research and Creativity, 2005
FSU Academic Senate, 2004

**College of Arts and Science**

Chair, Computer Science Department Chair Search Advisory Committee, 2008
Chair, Computer Science Department Chair Search Advisory Committee, 2004

**Department of Computer Science**

Member, PhD Portfolio Committee, 2008
Member, Faculty Recruitment Committee, 2008
Member, Computer Science Executive Committee, 2008
Member, PhD Portfolio Committee, 2007
Member, Computer Science Executive Committee, 2007
Chair, Computer Science Faculty Recruitment Committee, 2006
Member, Computer Science Executive Committee, 2005
Member, Computer Science Faculty Evaluation Committee, 2005
Member, PhD Portfolio Committee, 2005
Member, Faculty Recruitment Committee, 2004
Member, PhD Portfolio Committee, 2004
Member, Faculty Recruitment Committee, 2003
Member, Graduate Student Recruitment Committee, 2003
Member, PhD Portfolio Committee, 2003
Department Representative, Fall 2003 Commencement

## The Profession

**Editorial Board Membership(s)**

Editorial Board Member (*2000-2004*). *Journal of Instruction Level Parallelism*

## Conference, Symposia and Workshop Program Committee Membership(s)

Parallel Architecture and Compilation Techniques: 2000, 2008
Computer Design: 2005-2008
Compilers, Architecture, Synthesis for Embedded Systems, 2006, 2008
Languages, Compilers and Tools for Embedded Systems: 2008
INTERACT: 2007
High Performance Computer Architecture, 2001, 2007
Optimization for DSP and Embedded Systems 2004, 2007
Microarchitecture: 1996-2000

## Reviewer for Grant Applications

National Science Foundation Panel Member, 4 times total (2 times since joining FSU).