24th IEEE Symposium on Computer Arithmetic

ARITH 24

London, UK. July 24–26, 2017

Since 1969, the ARITH symposia have served as the flagship conference for presenting scientific work on the latest research in computer arithmetic. Authors are invited to submit papers describing recent advances on all aspects of computer arithmetic and its applications or implementations. This includes, but is not restricted to, the following topics:

- Foundations of number systems and arithmetic
- Arithmetic processor design and implementation
- Arithmetic algorithms and their analysis
- Floating-point units, algorithms, and numerical analysis
- Elementary and special function implementations
- Power-efficient or low-energy arithmetic units and processors
- Industrial implementation of arithmetic units and processors
- Test, validation, and formal verification techniques for arithmetic implementations
- Fault/error-tolerance in arithmetic implementations
- Arithmetic for FPGAs and reconfigurable logic
- Design automation for computer arithmetic implementations
- Computer arithmetic for security and cryptography
- Arithmetic to enhance accuracy or reliability (multiple-precision, interval arithmetic, …)
- Arithmetic challenges in HPC and exascale computing (accuracy, reproducibility, …)
- Arithmetic for specific application domains (big-data analytics, signal processing, computer graphics, multimedia, computer vision, finance, …)
- Computer arithmetic in emerging technologies
- Non-conventional computer arithmetic and applications

Symposium website: http://arithsymposium.org/

Submission site: https://easychair.org/conferences/?conf=arith24

Procedure for submission

A PDF version of the full paper should be submitted no later than **December 31st, 2016**. Papers under review elsewhere are not acceptable for submission to ARITH 24. By submitting a paper you implicitly confirm you are solely submitting it to ARITH 24. Authors will be notified of acceptance in March 2017, and final camera-ready papers will be due in May 2017.

Note on paper formatting

The final submissions of accepted papers cannot exceed 8 pages (**NO extra pages**) using the IEEE Computer Society Conference format (two columns). However, for review, authors may submit a paper with a maximum of 20 pages, 12pt font size, single column and double spacing.